iSBC 86/05™
SINGLE BOARD COMPUTER
HARDWARE REFERENCE MANUAL

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NOTE TO READERS

This hardware reference manual utilizes a visual scheme to denote section levels, rather than a numerical scheme used in many technical documents. This visual scheme allows you to more readily identify which section headings are sub-sections. Therefore, each section will have the same numbering convention throughout the manual (i.e., section 1-3, section 2-20, section 4-8). The visual distinction among the different sizes and the different fonts used for section headings indicate what level or order a particular section occupies. The following example illustrates how this system is used in this manual:

3-27. 8259A PIC PROGRAMMING ..... 1st Order Heading

3-28. INTERRUPT PRIORITY MODES ... 2nd Order Heading

3-29. FULLY NESTED MODE. In this .... 3rd Order Heading

By glancing through this manual before you start reading, the visual method of section ordering will become apparent. You may also refer to the Table of Contents on page vii, to see how the sections compare to each other. By using a visual system rather than a cumbersome numerical system, we hope to improve the readability of this manual, and thereby increase its usefulness.

PREFACE

This manual provides general information, installation and setup instructions, programming guidelines for the on-board, programmable devices, board level principles of operation, and service information for the iSBC 86/05 Single Board Computer. Related information is provided in the following publications:

- *The 8086 Family User's Manual,* Order No. 9800722.
- *The 8086 Primer,* by Stephen P. Morse. Hayden Book Company, Inc., Rochelle Park, N.J., 1980. ISBN: 0-8104-5165-4.
- *iSBC Applications Manual,* Order No. 142687.
- *Intel Multibus Specification,* Order No. 9800683.
- *Intel Multibus Interfacing,* Application Note AP-28A.
- *MCS-86 Assembly Language Programming Manual,* Order No. 9800640.
- *PL/M 86 Programming Manual,* Order No. 9800466.
- *Intel iSBX Bus Specification,* Order No. 142686.
- *Designing iSBX Multimodule Boards,* Application Note AP-96.
- *Using the iRMX 86 Operating System,* Application Note AP-86.
- *iSBC 337 Numeric Data Processor Hardware Reference Manual,* Order No. 142887.

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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 86/05 Single Board Computer is an Intel Multibus and iSBX Multimodule compatible, 16-bit computer system on a single printed circuit assembly (Figure 1-1). The iSBC 86/05 board includes an 8 MHz 8086-2 microprocessor, 8K bytes of on-board static random access memory (RAM), 24 programmable parallel I/O lines, one serial I/O port, three programmable interval timers, and a programmable interrupt controller. Sockets are provided for a maximum of 32K bytes of read only memory (ROM).

On-board memory expansion can be readily accomplished using plug-in memory expansion boards. On-board RAM size may be doubled, to 16K bytes using the optional iSBC 302 RAM Expansion Module. On-board ROM size may be increased to a maximum of 64K bytes, using the iSBC 341 ROM Expansion Module.

Additional on-board I/O capabilities are provided via the two iSBX Multimodule connectors on the iSBC 86/05 board. These connectors allow any of the optional Multimodule boards to be used on the iSBC 86/05 board.

This hardware reference manual provides the information you will need to promptly install and operate the iSBC 86/05 Single Board Computer. To optimize your application of this flexible board, we suggest reading the entire manual before attempting installation and operation.

1-2. DESCRIPTION

The iSBC 86/05 board is controlled by an Intel 8086-2 microprocessor operating at 8 MHz. Processor support is provided by an Intel 8284A Clock Generator - Driver and an Intel 8288 Bus Controller. The board can be jumpered to operate at 5 MHz, if necessary.

Up to 1 Megabyte of total system memory may be directly addressed by the iSBC 86/05 board. Of this amount, a maximum of 80K bytes may reside on-board (16K RAM + 64K ROM). The 8086 micro-

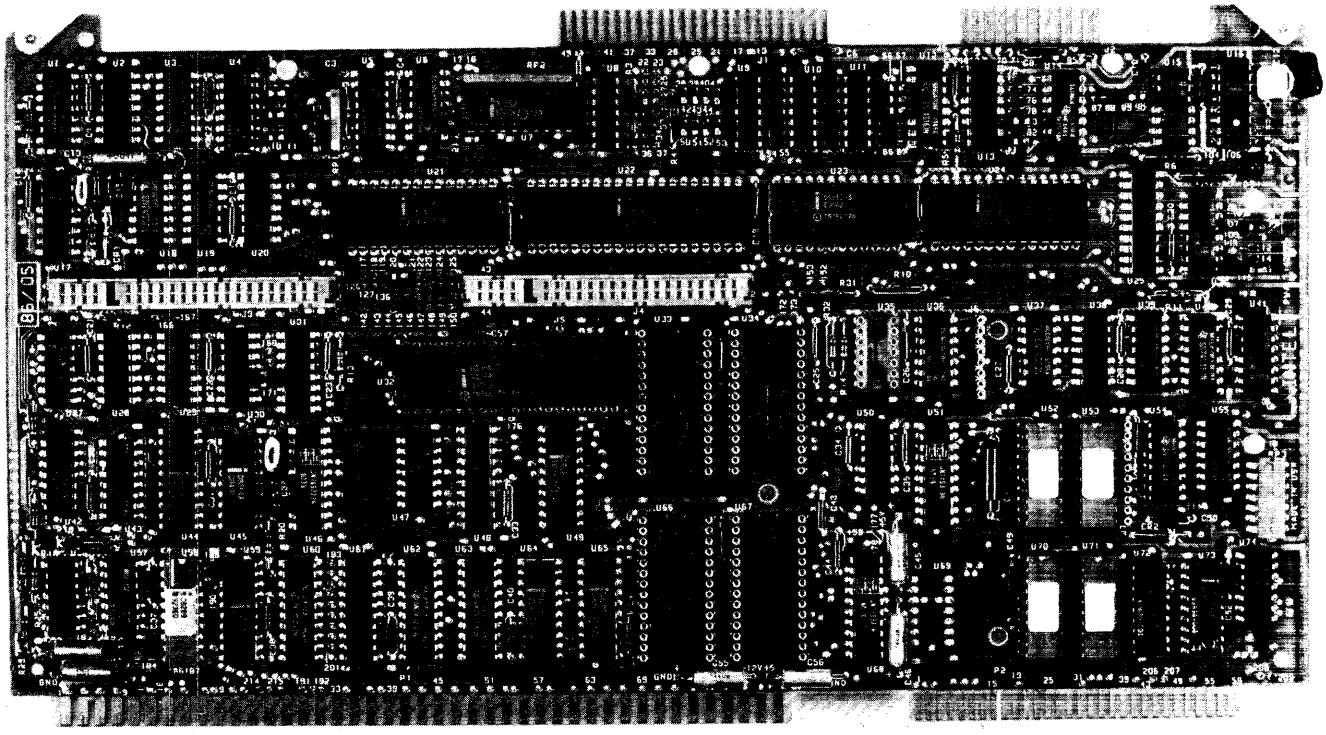


Figure 1-1. iSBC 86/05™ Single-Board Computer

processor can access either 8 or 16 bits of memory at a time, allowing maximum system compatibility.

The 8K bytes of on-board static RAM is implemented with four Intel 2168 (4K X 4 bit) static RAM devices. These high-speed devices require only a +5 volt supply, and are therefore well suited for battery backup applications. The iSBC 302 RAM Expansion Module increases the on-board RAM array to 16K bytes, using an additional four 2168 devices.

The board will accept a wide variety of ROM, PROM, and EPROM devices. Either 24 or 28-pin devices may be used. Four on-board sockets are provided, with expansion provided by the optional iSBC 341 ROM Expansion Module. Refer to Chapter 2 for complete information.

The on-board 8253-5 Programmable Interval Timer provides three independent counter outputs which may be configured to a variety of applications, including frequency output, rate generator, interval timer and real-time interrupts. One of the counters serves as the baud rate clock for the on-board 8251A Programmable Communications Interface device.

Serial I/O operation is handled by an Intel 8251 Programmable Communications Interface device. The board is configured to the RS 232C standard. However, this may be converted to a current loop TTY serial interface using optional equipment. Baud rates are software programmable using the on-board interval timer.

The iSBC 86/05 board utilizes one Intel 8255A-5 Programmable Peripheral Interface device to control the three, 8-bit, parallel I/O ports. All 24 lines may be configured to a variety of dedicated or general purpose applications. One port is equipped with an Intel 8287 Bus Transceiver. The other two ports are equipped with sockets for line drivers or terminators.

All interrupts, except the 8086-2 non-maskable interrupt (NMI), are handled by the on-board Intel 8259A Programmable Interrupt Controller device. System interrupts can be vectored to the interrupt controller via the Multibus lines, and additional interrupts may originate from one or two iSBX Multimodule boards. An on-board interrupt jumper matrix allows interrupt configuration flexibility and provides priority selection.

Two iSBX bus connectors (J3 and J4) are provided on the iSBC 86/05 board. These connectors are designed to expand the board's I/O functions, using special purpose optional iSBX Multimodule boards, such as the iSBX 350 Parallel I/O Multimodule Board. The Multimodule boards reside directly on the iSBC 86/05 board (Figure 1-2). One or two

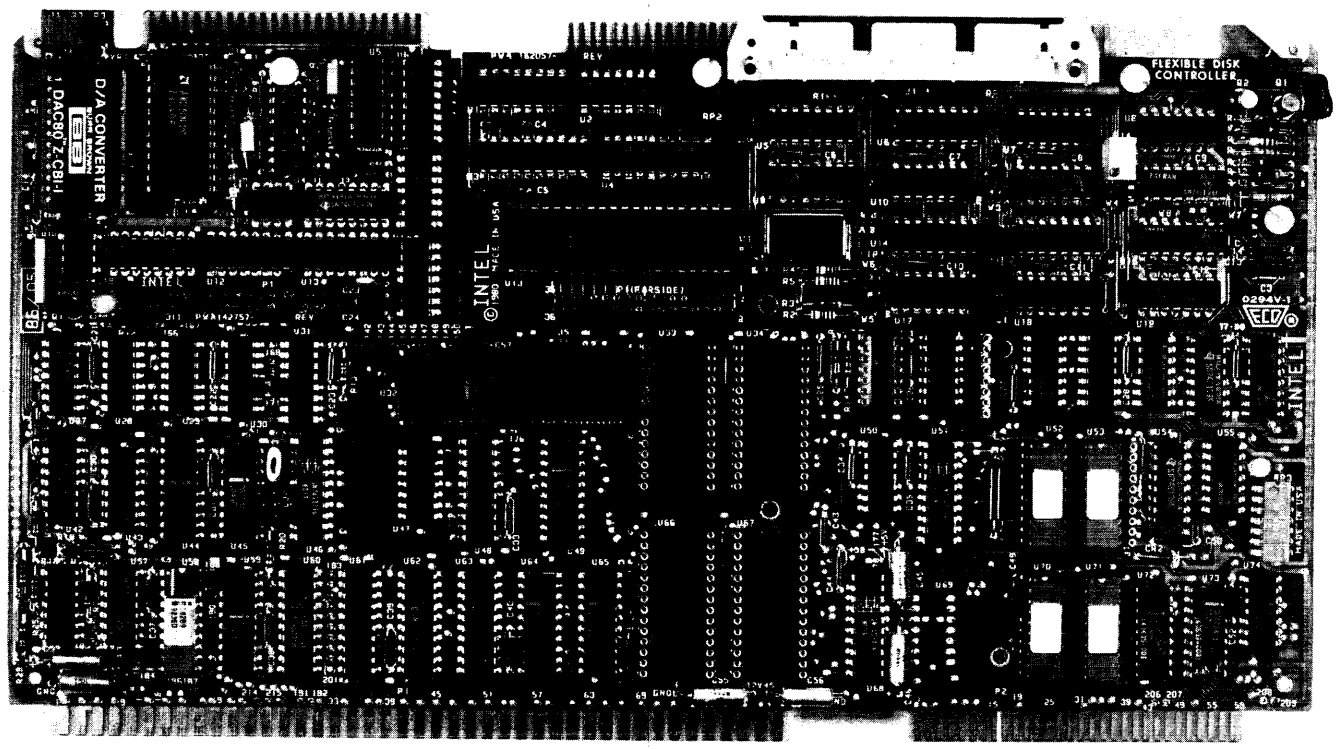


Figure 1-2. iSBC 86/05™ Board with Optional iSBX™ Multimodule Boards

Multimodules may be added, as required by your application.

Off-board system access is provided by the Multibus connector (P1) and an auxiliary connector (P2). Off-board peripheral operations are handled through 24 parallel I/O lines (connector J1), a serial communications channel (connector J2), and two iSBX Multimodule connectors.

The iSBC 86/05 board is designed to operate as a full master in any Intel Multibus compatible chassis or backplane. The board may also reside in your own custom chassis, using Multibus compatible connectors (refer to Chapter 2).

1-3. DOCUMENTATION SUPPLIED

Each iSBC 86/05 board is shipped with a corresponding set of schematic diagrams. These drawings should be inserted into the back of this manual for future reference. Refer to Chapter 5 for related information.

1-4. ADDITIONAL EQUIPMENT REQUIRED

The iSBC 86/05 board requires few optional components for basic operation. Depending on your application, you may need to purchase a parallel I/O connector, a serial I/O connector, and additional RAM if more than 8K bytes are required. Any on-board ROM must also be purchased separately. Chapter 2 provides information for selecting these items.

1-5. SPECIFICATIONS

Specifications of the iSBC 86/05 board are provided in Table 1-1.

Table 1-1. Board Specifications

CPU	Intel 8086-2
Operating Rate	8 MHz (default)
	5 MHz (optional)
Single Bus Cycle	125 nanoseconds
Minimum Processor Bus Cycle (four single cycles)	500 nanoseconds
MULTIBUS CLOCK	9.830 MHz (BCLK/ & CCLK/)
PCI Clock Input	2.458 MHz
PIT Input 0 & 2	1.229 MHz
PIT Input 1	153.6 KHz
RAM ACCESS TIME	85 nsecs max, Address to Data
ROM/PROM/EPROM ACCESS TIME	
8 MHz	285 - 660 nsecs (0 - 3 Waits)
5 MHz	520 - 1120 nsecs (0 - 3 Waits)
MEMORY CAPACITY	1M Byte (1,048,576 bytes)
Maximum On-Board ROM/EPROM	64K Bytes (65,536 bytes)
Maximum On-Board RAM	16K Bytes (16,384 bytes)
Remaining Off-Board Expansion	920K Bytes (966,656 bytes)
MEMORY ADDRESSING	All notation in hexadecimal
On-Board RAM	0 - 1FFF
With iSBC 302	0 - 3FFF
On-Board ROM	FE000 - FFFFF using 2716 devices
	FC000 - FFFFF using 2732 devices
	F8000 - FFFFF using 2764 devices
With iSBC 341 Expansion	FC000 - FFFFF using 2716 devices
	F8000 - FFFFF using 2732 devices
	F0000 - FFFFF using 2764 devices

Table 1-1. Board Specifications (Continued)

ON BOARD I/O ADDRESSING			
iSBC Connector J4 (8-bit)	80 - 9F Even Bytes Only		
iSBX Connector J4 (16-bit)	80 - 8F		
iSBX Connector J3 (8-bit)	A0 - BF Even Bytes Only		
iSBX Connector J3 (16-bit)	A0 - AF		
Interrupt Controller	C0 or C4 ICW1, OCW2, OCW3, Status, & Poll		
	C2 or C6 ICW2, ICW3, ICW4, & Masks		
Parallel Interface	C8 PPI Port A		
	CA PPI Port B		
	CC PPI Port C		
	CE PPI Control		
Interval Timer	D0 Counter 0		
	D2 Counter 1		
	D4 Counter 2		
	D6 Counter Control		
Serial Interface	D8 or DC Data		
	DA or DE Mode or Status		
INTERFACES			
Multibus	All signals TTL compatible		
Parallel I/O	All signals TTL compatible		
Interrupt Requests	All signals TTL compatible		
Interval Timer	All signals TTL compatible		
iSBX Bus	All signals TTL compatible		
Serial I/O	RS 232C compatible, data set		
ELECTRICAL REQUIREMENTS			
CONFIGURATION	**+5Vdc**	**+12Vdc***	**-12Vdc***
Standard Board, no ROM/EPROM	4.9A	25mA	23mA
Add for four 2716 devices	100mA	—	—
Add for four 2732 devices	150mA	—	—
Add for four 2764 devices	180mA	—	—
Add for iSBC 302 Option	1.08A	—	—
Add for iSBC 341 Option	1.80A	—	—
Add for each iSBX Multimodule	3.00A	1.0A	1.0A
Add for iSBC 337 Option	475mA	—	—
STANDBY CURRENT REQUIREMENTS			
Four 2716	25mA	—	—
Four 2732	30mA	—	—
Four 2764	30mA	—	—
iSBC 302 Option	180mA	—	—
iSBC 341 Option	180mA	—	—
BATTERY BACKUP REQUIREMENTS	0.8A	—	—
MAXIMUM OPERATING REQUIREMENTS (with all options)	12.2A	1.025A	1.025A

*+12Vdc and -12Vdc are required for RS232 applications only.

Table 1-1. Board Specifications (Continued)

PHYSICAL CHARACTERISTICS	
Width	12.00 in. (30.48 cm)
Length	6.75 in. (17.15 cm)
Thickness	0.50 in. (1.27 cm)
Weight	14 oz. (388 gram)
ENVIRONMENTAL CHARACTERISTICS	
Maximum Power Requirements	115 Watts
Maximum Heat Dissipation	1640 gcal/minute (6.63 Btu/minute)
Operating Temperature Range	0°C - 55°C
Operating Humidity Range	90% max non-condensing

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides specific information enabling you to install the iSBC 86/05 Single Board Computer into your system, with minimal effort. The board's default or factory configuration for RAM addressing, ROM/PROM size, and other variables is described, followed by procedures for altering the default configuration. In this manner the board will accommodate a variety of applications. To completely familiarize yourself with the flexibility of the iSBC 86/05 board, we recommend reading the entire chapter before installation and use.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment contact the Intel Product Service HOTLINE to obtain a return authorization number and further instructions (see Section 5-2). A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

2-3. INSTALLATION CONSIDERATIONS

There are several general requirements which should be considered prior to board installation and use. These requirements are discussed in Sections 2-4 through 2-6.

2-4. MINIMAL OPERATING REQUIREMENTS

The iSBC 86/05 board standard configuration is described in Chapter 1. In order to operate the board you may need additional equipment. For most applications this will typically be the following:

a. CPU software, residing in on-board ROM/PROM (Section 2-7).

b. I/O connectors and cables (Sections 2-28; 2-33; 2-34).

c. Additional on-board RAM, if more than 8K bytes are required (Section 2-9).

d. Line drivers or terminators for parallel I/O lines (Section 2-10).

Instructions for installing these items are provided in the sections listed above.

2-5. POWER REQUIREMENTS

Three voltages are required for operating the iSBC 86/05 board in most configurations: +5Vdc, +12Vdc, and -12Vdc. All must be within ±5% of absolute. However, some configurations do not require all voltages. Power requirements for the various board configurations are listed in Table 1-1. The table includes power required by any optional iSBX Multimodule boards which may be installed.

2-6. COOLING REQUIREMENTS

Operating temperature range for the iSBC 86/05 board is 0°C to 55°C. If the board is installed into an Intel system chassis, adequate cooling is provided by the fans supplied. However, if the board is used in another chassis, ensure adequate cooling is provided by taking temperature readings inside the chassis at the site environment.

2-7. ROM/PROM INSTALLATION

Sockets U33, U34 and U66, U67 are reserved for optional ROM/PROM devices. A maximum of 32K bytes may be installed in these four sockets, using four 16K byte 28-pin devices. A summary of compatible device types, capacity, and addressing is provided in Table 2-1. Device types may not be mixed, however empty sockets are allowed (provided they are not addressed).

Notice that ROM/PROM space is arranged into two banks (0 and 1), with each bank having a low byte and a high byte. When the 8086-2 CPU addresses a full 16-bit word, the low (or even) byte and the high (or odd) byte comprise the word. The CPU also has the capability to address either byte separately. Table 2-1 correlates the banks, bytes, socket numbers and addresses.

Before installing the devices on the board several jumper connections may be required to specify device size and power scheme. Table 2-2 specifies the board's factory default jumper configuration (set for 2716 devices) and summarizes the other possible ROM/PROM jumper connections.

CAUTION

Never install any device onto a board when power is applied. Damage to the board, device, and power supply could result.

CAUTION

The ROM/PROM sockets are 28-pin sockets which are used for both 24-pin and 28-pin devices. When inserting devices, ensure that pin 1 of the ROM/PROM device corresponds with pin 1 of the socket. Use the upper white dot for 28-pin devices and the lower white dot for 24-pin devices (Figure 2-1).

The bottom half of Table 2-1 provides address ranges when the optional iSBC 341 ROM/PROM Expansion Module is installed on the iSBC 86/05 board. This

Table 2-1. ROM/PROM Configurations

BANK NO: SOCKET NO: BYTE TYPE:	0 U66 LOW (EVEN) BYTES ONLY	1 U67 LOW (EVEN) BYTES ONLY	0 U33 HIGH (ODD) BYTES ONLY	1 U34 HIGH (ODD) BYTES ONLY	TOTAL ROM SPACE
DEVICE TYPE & SIZE:	ADDRESS RANGES				
2716 (2K x 8)	FE000- FEFFF	FF000- FFFFF	FE000- FEFFF	FF000- FFFFF	FE000- FFFFF
2732 (4K x 8)	FC000- FDFFF	FE000- FFFFF	FC000- FDFFF	FE000- FFFFF	FC000- FFFFF
2764 (8K x 8)	F8000- F8FFF	FC000- FFFFF	F8000- F8FFF	FC000- FFFFF	F8000- FFFFF
16K x 8	F0000- F7FFF	F8000- FFFFF	F0000- F7FFF	F8000- FFFFF	F0000- FFFFF

Address Ranges With iSBC 341 Module

BANK NO: SOCKET NO: BYTE TYPE:	3 U 5 LOW (EVEN) BYTES ONLY	2 U 6 LOW (EVEN) BYTES ONLY	3 U 2 HIGH (ODD) BYTES ONLY	2 U 3 HIGH (ODD) BYTES ONLY	TOTAL ROM SPACE
DEVICE TYPE & SIZE:	ADDRESS RANGES				
2716 (2K x 8)	FD000- FDFFF	FC000- FCFFF	FD000- FDFFF	FC000- FCFFF	FC000- FFFFF
2732 (4K x 8)	FA000- FBFFF	F8000- F9FFF	FA000- FBFFF	F8000- F9FFF	F8000- FFFFF
2764 (8K x 8)	F4000- F7FFF	F0000- F3FFF	F4000- F7FFF	F0000- F3FFF	F0000- FFFFF
16K x 8	E8000- EFFFF	E0000- E7FFF	E8000- EFFFF	E0000- E7FFF	E0000- FFFFF

Table 2-2. ROM/PROM Jumper Configurations

	DEVICE TYPE & SIZE			
	2716 2K x 8	2732 4K x 8	2764 8K x 8	16K x 8
U35 Jumpers	1 - 14 2 - 13 3 - 12	1 - 14 3 - 12 6 - 9	1 - 14 6 - 9	1 - 14 6 - 9 7 - 8
Decode PROM Jumpers	None	210 - 211	212 - 213	210 - 211 212 - 213

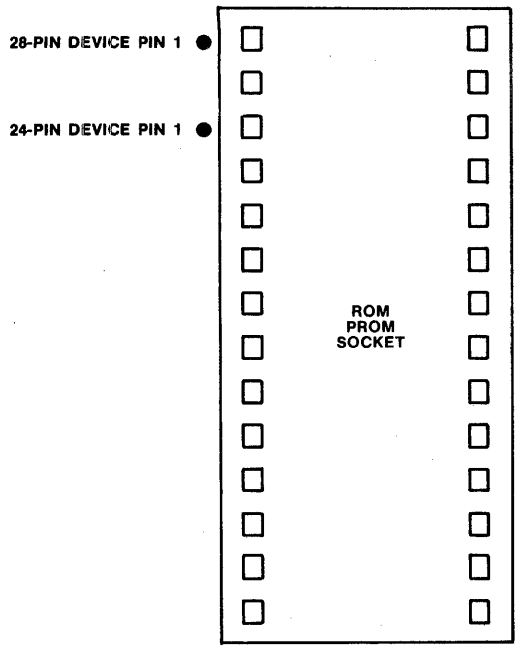


Figure 2-1. ROM/PROM Device Insertion

option should be installed only when your total on-board ROM/PROM requirements exceed 32K bytes. The addresses listed include ROM/PROM space already on the iSBC 86/05 board. Refer to Section 2-9 for iSBC 341 board installation information.

2-8. iSBC 341 MODULE INSTALLATION

The optional iSBC 341 ROM/PROM Expansion Module is designed to increase the amount of iSBC 86/05 on-board ROM/PROM. The size of the devices used on the module must match the size of the devices used on the board. For example, if the iSBC 86/05 board is equipped with 4K X 8 EPROM devices, the iSBC 341 module must also use 4K X 8 EPROM devices. The following procedure is recommended for iSBC 341 module installation:

a. Turn off power and remove iSBC 86/05 board from system.

b. Carefully remove ROM/PROM device from board socket U34 and install it into socket U1 on the iSBC 341 module. Similarly, remove the ROM/PROM device from board socket U67 and install it into socket U4 on the iSBC 341 module. Be sure to install these two devices in the sockets indicated. Byte order will be reversed if the ROM/PROM devices are incorrectly installed. Refer to CAUTION notice in Section 2-7 for related socket information.

c. Carefully insert all remaining ROM/PROM devices into the iSBC 341 module. Refer to CAUTION notice in Section 2-7 for related socket information.

d. Using the hardware supplied with the iSBC 341 module install it onto the iSBC 86/05 board as shown in Figure 2-2. The module connector fits directly into ROM/PROM sockets U34 and U67, and board connector J6.

e. Install jumper connection 105 - 106 on the iSBC 86/05 board.

f. Installation is complete. The iSBC 86/05 board is now ready to be installed into your system cardcage.

NOTE

To avoid using two cardcage slots when the iSBC 341 module is installed, place the iSBC 86/05 board in slot J2 (top slot).

2-9. iSBC 302 RAM MODULE INSTALLATION

The iSBC 86/05 board is shipped with 8K bytes of static RAM in place. Intel 2168 RAM devices are used in this configuration. The only means of expanding on-board RAM is by installing the optional iSBC 302 RAM Expansion Module. This will double the on-board RAM to 16K bytes. The following procedure is recommended for installing the RAM module:

a. Turn power off and remove the iSBC 86/05 board from its system.

b. Carefully remove the RAM devices from board sockets U53 and U71. Save these devices for use on the iSBC 302 module.

c. Using the hardware supplied with the iSBC 302 module, install the module onto the iSBC 86/05 board as shown in Figure 2-3. The iSBC 302 module connector pins fit directly into board sockets U53 and U71, and board connector J7. Ensure that all pins fit correctly before tightening the hardware.

d. Install the two RAM devices removed in step (b) into module sockets U1 and U4. Ensure pin 1 of the device matches pin 1 on the socket.

e. Install jumper 104 - 105 on the iSBC 86/05 board.

f. On-board RAM space with 16K bytes will cover 0 - 3FFF (hexadecimal) with the board in the default configuration.

g. Installation is complete. The iSBC 86/05 board is now ready to be installed into your system cardcage.

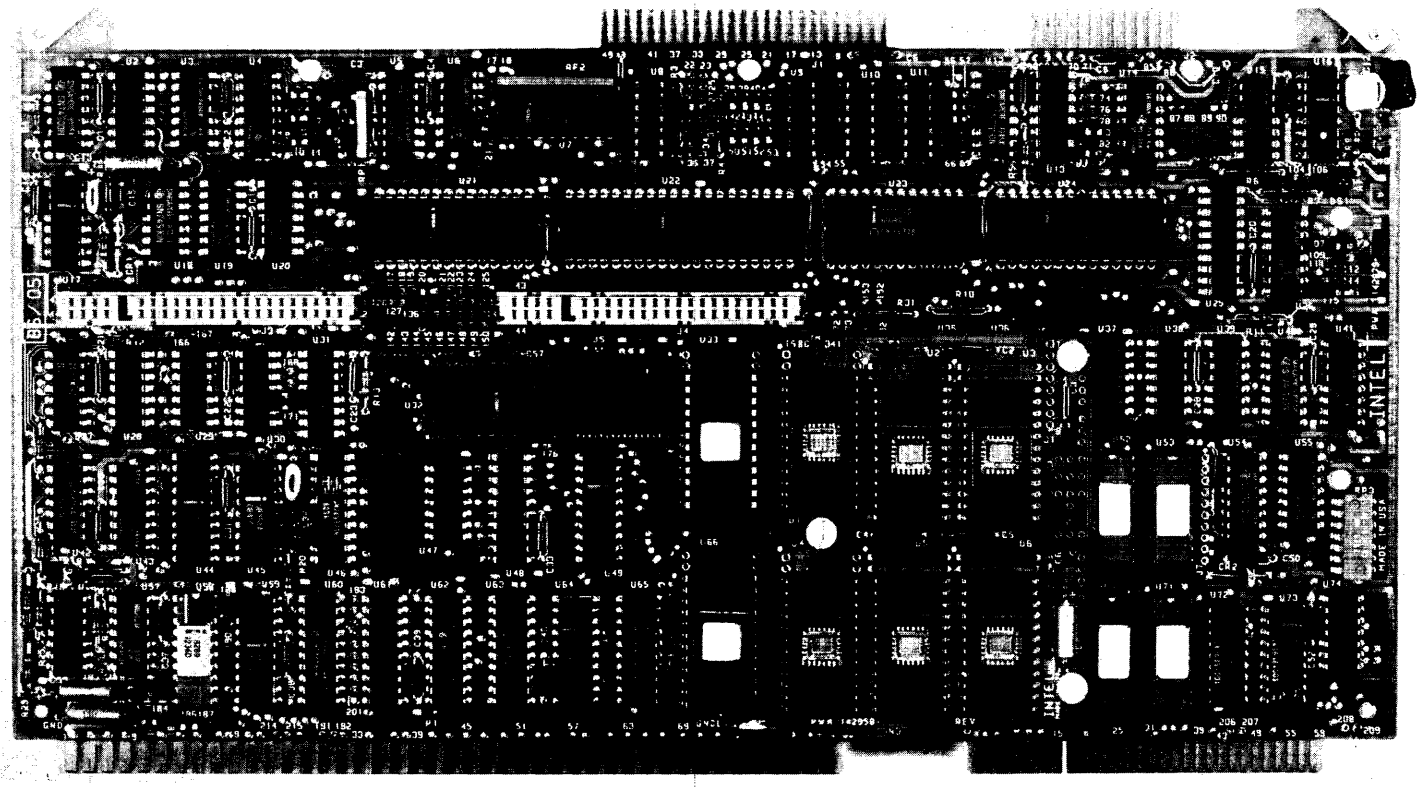


Figure 2-2. iSBC 341™ Module Insertion

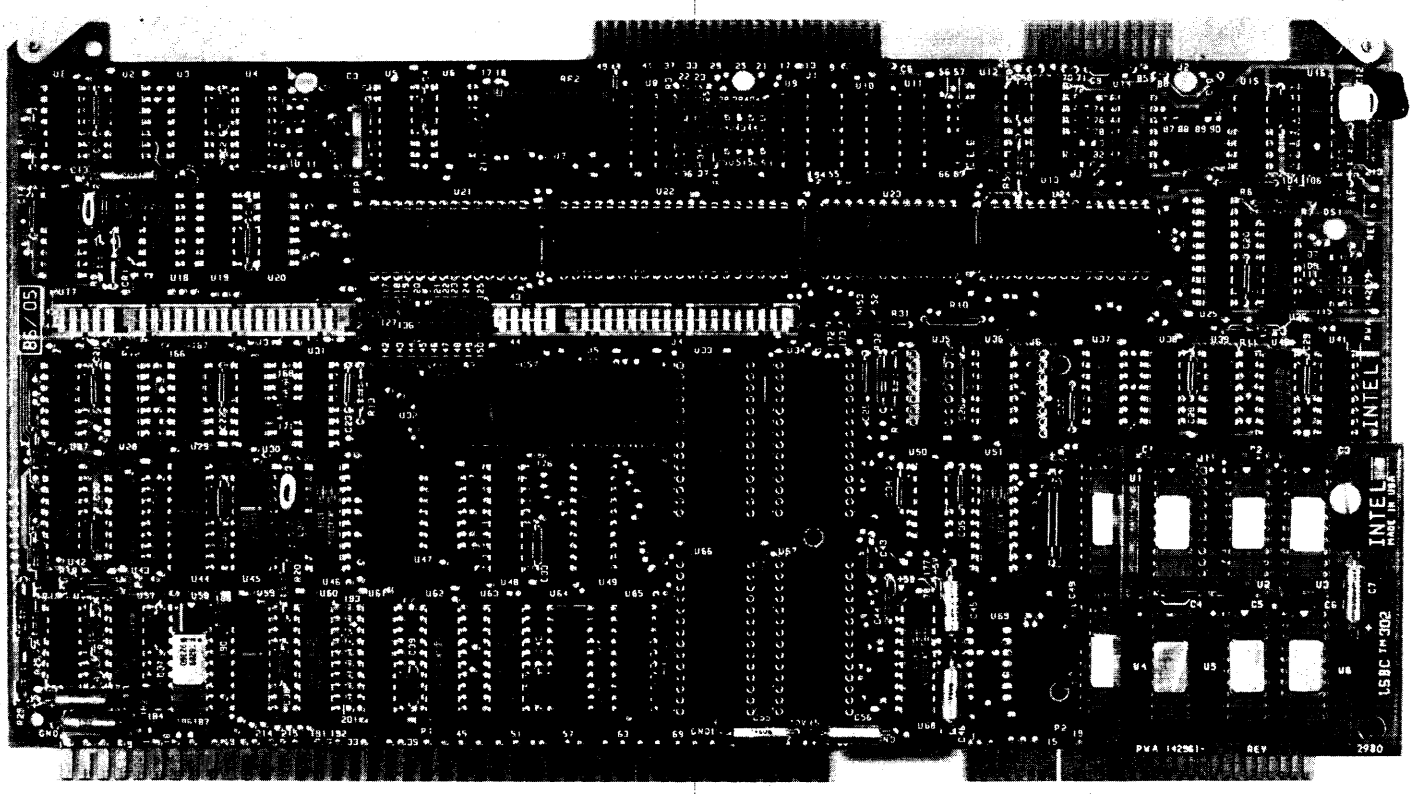


Figure 2-3. iSBC 302™ Module Insertion

NOTE

To avoid using two cardcage slots when the iSBC 302 module is installed, place the iSBC 86/05 board in slot J2 (top slot).

2-10. LINE DRIVERS AND I/O TERMINATORS

When using parallel ports CA and CC, line drivers or terminators are required for operation. The iSBC 86/05 board is equipped with a bidirectional bus transceiver on parallel port C8. Sockets U8 through U11 are provided for line driver/terminator devices. Table 2-3 lists the types of terminators and line drivers which are recommended for this purpose.

2-11. JUMPER CONFIGURATIONS

Much of the flexibility of your iSBC 86/05 board is due to the use of jumper connections which may easily be altered from their factory configurations to suit your particular application. Sections 2-12 through 2-23 describe optional jumper connections for all of the iSBC 86/05 configurations. Table 2-4 lists the factory default jumper connections on the board. Physical location of jumper posts on the board are shown in Figure 5-2. Jumper connections are also shown schematically in Figure 5-3.

Table 2-3. Line Driver and Terminator Circuits

Line Drivers	Current	I/O Terminators
7400 I	16 mA	iSBC 901
7403 I, OC	16 mA	
7408 NI	16 mA	iSBC 902
7409 NI, OC	16 mA	

I = inverting; NI = non-inverting; OC = open collector.

Table 2-4. iSBC 86/05 Factory Default

Figure 5-3 Schematic Sheet	Jumper Pair	Function
1	177-178	Battery Defeat
2	2-3	Wait State Generator
2	6-7	Wait State Generator
2	10-11	Wait State Generator
2	14-15	Failsafe Timer
2	19-20	PROM BUSY
2	170-171	TEST ONLY
2	181-182	8MHz Operation
4	179-180	BCLK/ To Multibus
4	183-184	CBRQ/ To Multibus
4	186-187	BPRO/ To Multibus
4	188-189	See Section 2-24
4	191-192	CCLK/ To Multibus
5	107-108	Page Address
5	115-116	Page Address
7	56-57	PIT Input CLK 2
7	58-59	PIT Input CLK 0
7	60-61	PIT Input CLK 1
7	79-80	RxC Input
7	83-84	TxC Input
7	89-90	OSC Output
7	91-92	DSR/ Input
8	25-27	PIT Gate 1 Control
8	28-29	Port C8 Direction
8	32-33	PIT Gate 0 Control
8	38-42	Port CC Bit 5
8	39-43	Port CC Bit 6
8	40-44	Port CC Bit 7
8	41-45	Port CC Bit 4
8	46-50	Port CC Bit 0
8	47-51	Port CC Bit 1
8	48-52	Port CC Bit 2
8	49-53	Port CC Bit 3
9	120-121	NMI Gate
9	123-124	Timer 0 INTR to IR2
9	125-132	51RxINTR to IR0
9	145-146	Multibus Interrupt IR5

2-12. INTERVAL TIMER JUMPER CONFIGURATIONS

The 8253-5 Programmable Interval Timer (PIT) is configured at the factory with three jumpers installed, as shown in Table 2-5. These three jumpers select the input frequencies to each of the three independent counters within the PIT. Outputs 0 and 1 from the timer are routed directly to the interrupt matrix (Section 2-16). These outputs may then be jumpered to the desired on-board interrupt level, or routed off-board via the Multibus interrupt lines, by connection to one of the outbound posts (194 through 201).

Output 2 is used for the 8251A Programmable Communications Interface (PCI) transmit and receive clocks.

2-13. SERIAL PORT JUMPER CONNECTIONS

The iSBC 86/05 board serial port is configured at the factory to the RS 232C standard interface. The board assumes the data set role. The serial port uses I/O connector J2. Jumper connections associated with the serial port are summarized in Table 2-6. Connector J2 pin assignments are provided in Table 2-7.

Table 2-5. Interval Timer Input Jumper Configurations

Function	Jumpers	Description
2.46 MHz	59 - 64	Optional input to CLK 0
	61 - 64	Optional input to CLK 1
	56 - 64	Optional input to CLK 2
1.23 MHz	58 - 59*	Default input to CLK 0
	56 - 57*	Default input to CLK 2
	57 - 61	Optional input to CLK 1
153.6 KHz	60 - 61*	Default input to CLK 1
Output 0	61 - 63	Optional cascade mode (see text)
Output 1	56 - 65	Optional cascade mode (see text)
Output 2	67 - XX	Optional cascade mode (see text)
External	62 - XX	Connect to 56, 59, 61 for external input (select one only)
Power Line Clock	66 - XX	Connect to 56, 59, 61 for 2X line frequency if using iSBC 665 Modular Chassis (select one)

NOTE: * indicates default connection; select one function per input only.

Table 2-6. Serial Port Jumper Configurations

Function	Jumpers	Description
On Board TxC	83 - 84*	Connects PIT outputs 2 to TxC
On Board RxC	79 - 80*	Connects PIT output 2 to RxC
External TxC	82 - 83	Connects J2-7 to TxC
External RxC	79 - 81	Connects J2-7 to RxC
Secondary TxC	72 - 73	Use with on board or external TxC clock.
Secondary TxD	73 - 74	Use with parallel port CC bit and STxC
	75 - 76	Connects STxD/STxC to J2-26
	76 - 78	Connects STxD/STxC to J2-5
	76 - 77	Connects STxD/STxC to J2-21
RTS/ to CTS/	87 - 88	Straps on board RTS/ to CTS/
Voltages	68 - 69*	Connects +5 Vdc to J2- 23
	85 - 86*	Connects +12 Vdc to J2 - 22
	70 - 71*	Connects -12 Vdc to J2 - 19
DSR Defeat	91 - 92*	Disconnects DSR input when removed

Note: * Indicates default connection installed.

Table 2-7. Connector J2 Pin Assignments

Pin No.	iSBC 86/05 Signal	RS-232C Pin No.	PCI Function
J2 - 1	Not Used	14	—
J2 - 2	Protective Ground	1	Ground
J2 - 3	Not Used	15	—
J2 - 4	Transmitted Data	2	RxD Input
J2 - 5	See J2 - 26[3]	16	See J2 - 26
J2 - 6	Received Data	3	TxD Output
J2 - 7	External Clock	17	TxC/RxC Input
J2 - 8	Request To Send	4	CTS/ Input
J2 - 9	Not Used	18	—
J2 - 10	Clear To Send	5	RTS/ Output
J2 - 11	Not Used	19	—
J2 - 12	Data Set Ready	6	DSR/ Input
J2 - 13	Data Terminal Ready	20	DTR/ Output
J2 - 14	Signal Ground	7	GND
J2 - 15	Not Used	21	—
J2 - 16	Not Used	8	—
J2 - 17	Not Used	22	—
J2 - 18	Not Used	9	—
J2 - 19	-12 Vdc[3]	23	—
J2 - 20	Not Used	10	—
J2 - 21	See J2 - 26[3]	24	See J2 - 26
J2 - 22	+12 Vdc[3]	11	—
J2 - 23	+5 Vdc[3]	25	—
J2 - 24	Not Used	12	—
J2 - 25	Ground	—	GND
J2 - 26	Secondary TxD or Clock Out[3]	13	STxD or TxC/TxD

Notes:
1. Odd numbered pins are on component side of board; even pins on solder side.
2. Cable connector numbering convention may not correspond with J2 numbering.
3. Not Connected at Factory.

2-14. PARALLEL PORT JUMPER CONFIGURATIONS

Parallel port CC has a jumper matrix between the 8255A-5 PPI device and the driver/terminator sockets U8 and U9. This arrangement allows a greater amount of flexibility when using these lines. Parallel port C8 has an 8287 Bus Transceiver installed in socket U7. The transceiver control line is configured at the factory for the output mode. Refer to Section 2-15 for instructions on converting this mode. Parallel port CA operation is determined entirely by software programming and the type of devices installed in sockets U10 and U11. Refer to Table 3-18 for a list of operating modes which are allowed for each parallel port.

Table 2-8 provides the default connections for all parallel ports, and shows the corresponding input/ output connector pin numbers. Table 2-9 provides jumper information and descriptions of the optional features associated with the port CC jumper matrix. Table 2-10 is a comprehensive guide to mode restrictions and jumper connections for all three parallel ports.

Before configuring the parallel ports for your application, refer to Section 3-22 for 8255A-5 programming information.

Table 2-8. Parallel Port Default Jumper Connections

Port CC Bit	Mode/Direction	Jumper Conn.	J1 Pin Number
0	0 Input	46 - 50	J1 - 24
1	0 Input	47 - 51	J1 - 22
2	0 Input	48 - 52	J1 - 20
3	0 Input	49 - 53	J1 - 18
4	0 Input	41 - 45	J1 - 26
5	0 Input	38 - 42	J1 - 28
6	0 Input	39 - 43	J1 - 30
7	0 Input	40 - 44	J1 - 32
Note: Driver/Terminators not installed at factory.			

Port C8 Bit	Mode/Direction	Jumper Conn.	J1 Pin Number
0	0 Output	NONE	J1 - 48
1	0 Output		J1 - 46
2	0 Output		J1 - 44
3	0 Output		J1 - 42
4	0 Output		J1 - 40
5	0 Output		J1 - 38
6	0 Output		J1 - 36
7	0 Output		J1 - 34
Note: For other modes see Section 2-14.			

Port CA Bit	Mode/Direction	Jumper Conn.	J1 Pin Number
0	0 Input	NONE	J1 - 16
1	0 Input		J1 - 14
2	0 Input		J1 - 12
3	0 Input		J1 - 10
4	0 Input		J1 - 8
5	0 Input		J1 - 6
6	0 Input		J1 - 4
7	0 Input		J1 - 2
Note: Driver/Terminators not installed at factory.			

2-15. PORT C8 TRANSCEIVER CONVERSION

Port C8 is equipped with an 8287 Bus Transceiver installed in socket U7. The transceiver is default connected to operate in the output only mode, with jumper 28 - 29. Two other modes are possible for the transceiver:

a. *Input only mode:* remove 28 - 29 and install 27 - 28.

b. *Programmable mode:* remove 28 - 29 or 27 - 28 and install a jumper between post 28 and the bit you select from port CC. (Connect to post on device side of port CC matrix.) The transceiver's direction or mode is then controlled by outputting the appropriate bit state to the device.

   a. out = output only mode

   b. out = input only mode

Table 2-9. Parallel Port CC Jumper Configurations

Function	Jumpers	Description
OUTPUTS:		
EXT CLK/	23 - XX	Connect to desired jumper post on connector side of parallel matrix; driver terminator socket must have terminator. See Table 2-5 for required timer jumper installation.
OVERRIDE/	24 - XX	Software programmable Multibus override control. Connect to desired bit on device side of parallel matrix.
SECONDARY TxD	22 - XX	Software programmable transmit channel. Connect to desired bit on device side of parallel matrix.
PA INTR	34 - XX	Parallel port interrupt "A". Software programmable on board interrupt. Connect to desired bit on device side of parallel matrix. See Table 2-11 for associated required jumper connection.
PB INTR	30 - XX	Parallel port interrupt "B". Software programmable on board interrupt. Connect to desired bit on device side of parallel matrix. See Table 2-11 for associated required jumper connection.
TEST/	35 - XX	Software programmable TEST/ input. When asserted, causes the 8086 to either execute WAIT states or become idle.
BUS INTR OUT	31 - XX	Software programmable Multibus (System) interrupt output. Requires additional connection from jumper post 193 to desired **output post** (194 through 201). See Schematic sheet 9 for levels.
GATE 0 CNTRL	33 - XX	Software programmable gate input for 8253A PIT. Connect to desired bit on device side of parallel matrix.
GATE 1 CNTRL	25 - XX	Software programmable gate input for 8253A PIT. Connect to desired bit on device side of parallel matrix.
NMI MASK/	26 - XX	Software programmable means to switch the 8086 NMI input on or off. A low disables the NMI input gate. Connect to desired bit on device side of parallel matrix.
DS1	54 - 55	Software programmable indicator lamp. Lamp is connected to bit 3 of port CC. Install jumper to enable.
PORT C8 DIRECTION	28 - XX	Controls direction (input or output) of port C8. Refer to Section 2-15.
INPUT:		
PFSN/	36 - XX	Power fail sense line. This line is an output from an off-board latch which indicates a power failure has occurred. PFSN/ may be ready by the parallel port, in conjunction with a battery backup power-on sequence. Refer to Section 2-32. Connect post 37 to one of the available input lines.

Note: XX denotes variable bit choice. Only one function per bit is allowed.

Table 2-10. Parallel Port Jumpers & Restrictions

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
C8	0 Input	8287: U7	*28-29	28-32	8287 = input enabled.	CA	None; can be mode 0 or 1, input or output.
						CC	None; can be in mode 0, input or output, unless Port CA is in Mode 1.
C8	0 Output (latched)	8287: U7		*28-29	8287 = output enabled.	CA	None; can be in Mode 0 or 1, input or output.
						CC	None; can be in Mode 0, input or output, unless Port CA is in Mode 1.

*Default jumper connected at the factory.

Table 2-10. Parallel Port Jumpers & Restrictions (Continued)

Port	Mode	Driver (D) Terminator (T)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
C8	1 Input (strobed)	8287: U7 T: U8 D: U9	*28-29	28-32	8287 = input enabled.	CA	None; can be in mode 0 or 1, input or output.
				*41-45	Connects J1-26 to STB_A/ input.	CC	Port CC bits perform the following:
			*38-42 and *49-53	42-49	Connects IBF_A output to J1-18.		• Bits 0, 1, 2 — Control for Port CA if Port CA is in Mode 1.
				34-53	Connects INT_A output to		• Bit 3 — Port C8 interrupt jumper matrix.
							• Bit 4 — Port C8 Strobe (STB/) input.
							• Bit 5 — Port C8 Input Buffer Full (IBF) output.
							• Bits 6, 7 — Port CC input or output (both, must be in same direction).
C8	1 Output (latched)	8287: U7 T: U8 D: U9		*28-29	8287 = output enabled.	CA	None; can be in Mode 0 or 1, input or output.
				*39-43	Connects J1-30 to ACK_A/ input.	CC	Port EA bits perform the following:
			*49-53 and *40-44	44-49	Connects OBF_A output to J1-18.		• Bits 0, 1, 2 — Control for Port CA if Port CA is in Mode 1.
				34-53	Connects INT_A output to interrupt matrix.		• Bit 3 — Port C8 interrupt (PA INTR) to interrupt jumper matrix.
							• Bits 4, 5 — Port CC input or output (both must be in same direction).
							• Bit 6 — Port C8 Acknowledge (ACK/) input.
							• Bit 7 — Port C8 Output Buffer Full (OBF/) output.
C8	2 (bidirectional)	8287: U7 T: U8 D: U9	*28-29	39-29	Allows ACK_A/ input to control 8287 in/out direction.	CA	None; can be in Mode 0 or 1, input or output.
						CC	Port CC bits perform the following:
				*41-45	Connects J1-26 to STB_A/ input.		• Bit 0 — Can only be used for jumper option.
			*38-42 and *46-50	42-46	Connects IBF_A output to J1-24.		• Bits 1, 2 — Can be used for input or output if Port CA is in Mode 0.

*Default jumper connected at the factory.

Table 2-10. Parallel Port Jumpers & Restrictions (Continued)

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
				*39-43	Connects J1-30 to ACK_A/ input.		• Bit 3 — Port C8 Interrupt (PA INTR) to interrupt jumper matrix.
			*40-44 and *49-53	44-49	Connects OBF_A/ output to J1-18.		• Bit 4 — Port C8 Strobe (STB/) input.
				34-53	Connects INT_A output to interrupt matrix.		• Bit 5 — Port C8 Input Buffer Full (IBF) output.
							• Bit 6 — Port C8 Acknowledge (ACK/) input.
							• Bit 7 — Port C8 Output Buffer Full (OBF/) output.
CA	0 Input	T: U10, U11	None	None		C8	None.
						CC	None; Port CC can be in Mode 0, input or output, if Port C8 is also in Mode 0.
CA	0 Output (latched)	D: U10, U11	None	None		C8	None
						CC	None; Port CC can be in Mode 0, input or output, if Port C8 is also in Mode 0.
CA	1 Input (strobed)	T: U8, U10, U11 D: U9		*47-51	Conencts IBF_B output to J1-22.	C8	None.
						CC	Port CC bits perform the following:
			*40-44 and *48-52	40-52	Connects J1-32 to STB_B/ input.		• Bit 0 — Port CA Interrupt (PB INTR) to interrupt jumper matrix.
				30-50	Connects INT_B output interrupt matrix.		• Bit 1 — Port CA Input Buffer Full (IBF) output.
							• Bit 2 — Port CA Strobe (STB/) input.
							• Bit 3 — If Port C8 is in Mode 0, bit 3 can be input or output. Otherwise, bit 3 is reserved.
							• Bits 4, 5, 6, 7 — Depends on Port C8 mode.
CA	1 Output (latched)	T: U8 D: U9, 10, 11		*42-51	Connects OBF_B/ output J1-22.	C8	None.
						CC	Port CC bits perform the following:
			*40-44 and *48-52	40-52	Connects J1-32 to ACK_B/ input.		• Bit 0 — Port CA interrupt (PB INTR) to interrupt jumper matrix.
			*46-50	30-50	Connects INT_B output to interrupt matrix.		• Bit 1 — Port CA Output Buffer Full (OBF/) output.

*Default jumper connected at the factory.

Table 2-10. Parallel Port Jumpers & Restrictions (Continued)

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
							• Bit 2 — Port CA Acknowlege (ACK/) input. • Bit 3 — If Port C8 is in Mode 0, bit 3 can be input or output. Otherwise, bit 3 is reserved. • Bit 4, 5, 6, 7 — Depends on Port C8 mode.
CC (upper)	0 Input	T: U8	None	41-45 *38-42 *39-43 *40-44	Connects bit 4 to J1-26. Connects bit 5 to J1-28. Connects bit 6 to J1-30. Connects bit 7 to J1-32.	C8	Port C8 must be in Mode 0 for all four bits to be available.
						CA	Port CA must be in Mode 0 for all four bits to be available.
CC (lower)	0 Input	T: U9	None *47-51	*46-50 *47-51 *48-52 *49-53	Connects bit 0 to J1-24. Connects bit 1 to J1-22. Connects bit 2 to J1-20. Connects bit 3 to J1-18.	C8	Port C8 mustbe in Mode 0 for all four bits to be available.
						CA	Port CA must be in Mode 0 for all four bits to be available.
CC (upper)	0 Output (latched)	D: U8	None	Same as for Port CC (upper) mode 0 Input.		C8	Same as for Port CC (upper Mode 0 Input.
CC (lower)	0 Output (latched)	D: U9	None	Same as for Port CC (lower) Mode 0 Input.		CA	Same as for Port CC (lower) Mode 0 Input.
*Default jumper connected at the factory.							

2-16. INTERRUPT MATRIX JUMPER CONFIGURATIONS

The iSBC 86/05 board provides jumper posts for 12 on-board interrupt sources and 11 off-board sources. Any eight of these sources can be interfaced to the 8259A Programmable Interrupt Controller (PIC) through the on-board interrupt matrix. The PIC provides eight interrupt levels. In addition the 8086 CPU can utilize its NMI input for high priority interrupt requests.

In the factory default configuration, the following four interrupt matrix jumpers are installed:

a. 123 - 124 Timer 0 output to IR2 on PIC

b. 145 - 146 Multibus interrupt INT5/ to IR5 on PIC

c. 120 - 121 Disable NMI Mask gate

d. 125 - 132 RxRDY Interrupt

Table 2-11 provides a complete list of possible interrupt jumper configurations on the iSBC 86/05 board. Refer to Section 3-27 for 8259A programming information.

In addition, the iSBC 86/05 board will support Multibus vectored interrupts from off-board slave 8259A interrupt controllers. Refer to Section 2-17 for information on Multibus vectored interrupts.

The following sections provide brief descriptions of all interrupt request lines which are part of the interrupt matrix or related to the iSBC 86/05 board interrupt structure.

iSBX™ Multimodule Interrupt (SBX1 INT0,1; SBX2 INT0,1)

Two interrupt request lines are available for each iSBX Multimodule board installed on the iSBC 86/05 board.

Interval Timer Outputs (TIMER0,1 INTR)

These two lines come directly from the 8253A Interval Timer. The timer 0 line is jumpered at the factory to interrupt request line INT2 (123 - 124). The timer 1 output is not connected at the factory.

Table 2-11. Interrupt Matrix Jumper Configurations

MATRIX INPUTS	DESCRIPTION	JUMPER POSTS		MATRIX OUTPUTS
		IN	OUT	
iSBX 2 INT0	J3 Multimodule INT 0	117	132	INT0 Input
iSBX 2 INT1	J3 Multimodule INT 1	126		
iSBX 1 INT0	J4 Multimodule INT 0	137		
iSBX 1 INT1	J4 Multimodule INT 1	138		
			133	INT1 Input
TIMER0 INTR	PIT Output 0	123		
TIMER1 INTR	PIT Output 1	122		
PA INTR	Parallel Port INT A	141	124	INT2 Input
PB INTR	Parallel Port INT B	140		
51TxINTR	PCI Transmit INT	134		
51RxINTR	PCI Receive INT	123	131	INT3 Input
PLC	Power Line Clock	150		
MINT	8087 Math Chip INT	139		
PFIN/	Power Fail INT	118	130	INT4 Input
EXT INTR0	External INT from J1-50	119		
EDGE INTR	Edge Sensitive Mode INT	129		
INT0/	Multibus INT from P1-41	144	145	INT5 Input
INT1/	Multibus INT from P1-42	136		
INT2/	Multibus INT from P1-39	142		
INT3/	Multibus INT from P1-40	143	128	INT6 Input
INT4/	Multibus INT from P1-37	147		
INT5/	Multibus INT from P1-38	146		
INT6/	Multibus INT from P1-35	149	127	INT7 Input
INT7/	Multibus INT from P1-36	148		
GND	Ground	121	120	NMI Gate

Note. Connect the desired IN jumper post to the desired OUT post. The following jumpers are factory installed. 123 - 124; 145 - 146; 120 - 121; and 125 - 132.

Table 2-11A. Multibus™ Interrupt Output Jumper Configurations

OUTPUT LINE	P1 PIN	JUMPER POST	BUS INTR OUT POST
INT0/	P1-41	199	
INT1/	P1-42	201	
INT2/	P1-39	195	
INT3/	P1-40	197	193
INT4/	P1-37	194	
INT5/	P1-38	196	
INT6/	P1-35	200	
INT7/	P1-36	198	

Note. Connect one jumper only from desired Multibus jumper post to the Bus Interrupt Output post (193). This option also requires a parallel port jumper matrix connection — see Section 2-16.

Parallel Port Interrupts A, B (PA INTR & PB INTR)

Essentially these two lines are software programmable interrupt lines. Connect each line to the desired interrupt request input. Refer to Section 2-13 for instructions on installing the parallel port matrix jumpers required for this option.

Transmit and Receive Interrupts (51TxINTR & 51RxINTR)

These signals originate at the 8251A Programmable Communications Interface (PCI) device. The signal 51TxINTR is equivalent to TxRDY on the PCI and when true indicates that the PCI is ready to accept a date character from the CPU. Likewise, 51RxINTR is equivalent to RxRDY and when true indicates that the PCI contains a data character to be read by the CPU. Refer to the Intel Component Data Catalog for additional PCI information.

Power Line Clock (PLC)

This external signal is supplied by the iSBC 665/666 Modular Chassis, or similar circuit. It enters the board via auxiliary connector pin P2-31 and is specified at 120 Hz (double the AC line frequency).

Math Interrupt (MINT)

This signal originates from the optional iSBC 337 Numeric Data Processor Multimodule board. This interrupt is used only in conjunction with this option.

Power Fail Interrupt (PFIN/)

Furnished by the iSBC Power Supply (or equivalent), this signal indicates that an AC line power failure has occurred and DC voltage loss is imminent. Typically, this signal is jumpered to the NMI input on the 8086 CPU and is used in conjunction with a user written power down routine and battery backup scheme. Refer to Section 2-32 for additional battery backup information.

External Interrupt 0 (EXT INTR0)

This external interrupt signal enters the board via parallel port connector P1-50. The incoming signal is inverted by the iSBC 86/05 board, therefore a low state will activate the interrupt request (level mode), or a high to low transition (edge sensitive mode).

Single Request Edge Sensitive Feature (EDGE INTR)

The iSBC 86/05 board is equipped with special circuitry which allows you to operate a single interrupt request line in the edge sensitive mode, while the 8259A Interrupt Controller is in the level or edge mode. This feature is extremely useful when you want the interrupt controller to operate in the level sensitive mode, but a critical request typically expires before the controller can acknowledge or service the request. For example, you could jumper the on-board failsafe timer output to this circuit, to call a specific time-out routine, or alarm.

To enable EDGE INTR, two jumper connections are required: first install a jumper from the desired request line to jumper post 13 (edge converter circuit input); then install a jumper between interrupt matrix post 129 and the desired interrupt controller input post. To implement the failsafe timer example described above, install the first jumper between posts 14 - 15 and then install the jumper to the desired interrupt controller input. Refer to Section 2-22 for additional failsafe timer information.

Non-Maskable Interrupt Input Mask

The 8086 CPU NMI input may be configured to be software selectable. This is called the Non-Maskable Interrupt Input Mask on the iSBC 86/05 board. Two jumper connections are required to enable this option: first, remove jumper connection 120 - 121 and install a jumper between interrupt matrix post 120 and the desired interrupt source (i.e., PFIN/). Then install another jumper between post 26 and the desired parallel port CC bit post. A high state on this line will enable the mask gate. A low state will disable the mask gate, preventing any non-maskable interrupts from reaching the 8086 CPU.

Multibus Interrupt Output Option (BUS INTR OUT)

The iSBC 86/05 board has an optional parallel port configuration which provides a software programmable interrupt output. This would allow you to issue an interrupt request on a system Multibus line with one of the parallel port CC bits. Two connections are required for this scheme: one jumper connection from the desired port CC bit to jumper post 31 and another jumper connection from jumper post 193 and the desired Mutibus Interrupt Line. Refer to Tables 2-9 and 2-11.

2-17. MULTIBUS VECTORED INTERRUPTS

The iSBC 86/05 board has the capability to service interrupt requests which originate with a request to a slave, off-board 8259A Programmable Interrupt Controller (PIC). The slave INTR output is connected to the master PIC on the iSBC 86/05 board via the Multibus lines, as shown in Figure 2-4. This type of interrupt request is called a Bus Vectored Interrupt. In general, a bus vectored interrupt should be of lower priority than interrupt requests which are input directly to the master PIC. The iSBC 86/05 board is configured at the factory to accept bus vectored interrupts. To disable this feature, you must install jumper 168 - 169.

Figure 2-4 shows, as an example, the on-board PIC (master) interfaced with two slave PIC devices. This arrangement leaves the master PIC with six inputs (IR2 through IR7) that can be used to handle the various on-board interrupt functions. The example scheme is implemented by programming the master PIC to handle IR0 and IR1 as bus vectored interrupts.

Each interrupt input (IR0 through IR7) to the master PIC may be individually programmed to be bus vectored or non-bus vectored. In the bus vectored mode, the slave PIC generates the restart address, and in the non-bus vectored mode the master PIC generates the restart address.

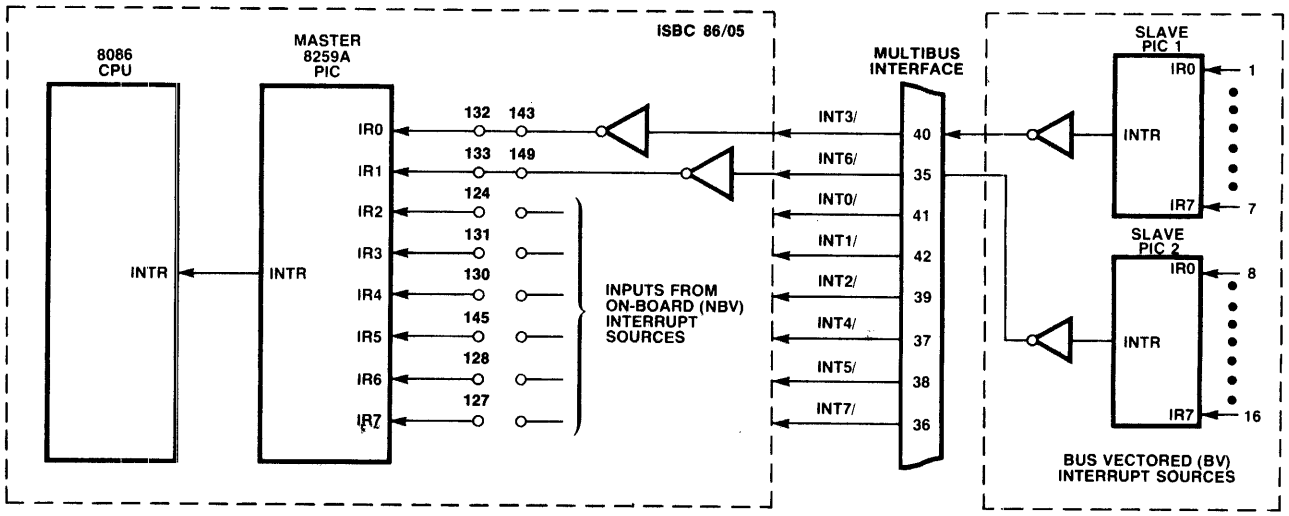


Figure 2-4. Simplified Master/Slave PIC Interconnect Example

Slave PIC devices must be identified as such during their initialization sequences (with ICW3). The master PIC must also be initialized to support slave PIC devices. Section 3-27 describes 8259A programming and provides initialization examples.

2-18. PAGE SELECT JUMPER CONFIGURATION

The iSBC 86/05 board is configured at the factory to recognize two separate on-board 128K byte pages as valid memory addresses. All on-board RAM must reside in an EVEN page, and all on-board ROM/PROM must reside in an ODD page. Any address within either page is recognized as a valid memory address by the decoding circuitry. The first page range is from address 0 - 1FFFF (hexadecimal) and the second is from E0000 - FFFFF. These pages may be altered by jumper selection as shown in Table 2-12.

2-19. SYSTEM CLOCK JUMPER SELECTION

The iSBC 86/05 board is configured at the factory to operate at 8 MHz. Alternatively, the board may be operated at 5 MHz, by jumper selection. To convert to 5 MHz operation, remove jumper 181 - 182.

2-20. BUS CLOCK AND CONSTANT CLOCK SELECTION

Bus Clock (BCLK/) and Constant Clock (CCLK/) are standard Multibus signals, common to most Intel iSBC boards. CCLK/ is the inverted version of BCLK/. Each signal operates at 9.83 MHz. The following table provides BCLK/ and CCLK/ jumper information:

Signal	Jumpers In	Multibus Pin
BCLK/	179 - 180*	P1 - 13
CCLK/	191 - 192*	P1 - 31

Table 2-12. Page Select Jumpers

Function	Address Range	Jumper Connection
RAM ONLY	00000 - 1FFFF	108 - 107 *
ROM/PROM ONLY	20000 - 3FFFF	110 - 107 or 115
RAM ONLY	40000 - 5FFFF	109 - 107 or 115
ROM/PROM ONLY	60000 - 7FFFF	112 - 107 or 115
RAM ONLY	80000 - 9FFFF	111 - 107 or 115
ROM/PROM ONLY	A0000 - BFFFF	114 - 107 or 115
RAM ONLY	C0000 - DFFFF	113 - 107 or 115
ROM/PROM ONLY	E0000 - FFFFF	116 - 115 *

Note: * indicates factory default connection. Select any two pages; connect first page jumper post to post 107; second page to post 115.

Either signal may be disabled by removing the appropriate jumper connections.

2-21. WAIT STATE GENERATOR SELECTION

The iSBC 86/05 board utilizes a wait state generator to allow the 8086 processor to wait for on-board addressed devices. Wait states are generated for all PROM, I/O, and interrupt requests. The number of wait states for each function is jumper selectable, allowing maximum utilization of processor time according to your system configuration. Table 2-13 provides the possible jumper configurations for the wait state generator and provides the maximum address to data times for each function.

2-22. FAILSAFE TIMER SELECTION

If non-existent off-board memory or I/O is accidently addressed by the 8086 CPU, the iSBC 86/05 board will execute wait states indefinitely, causing the board to cease processing. An on-board failsafe timer can be jumper selected to prevent this. The failsafe timer expires after a delay of approximately 10 milliseconds, giving the CPU a "false" READY signal so that it may resume processing. To enable the failsafe timer, install jumper connection 14 - 15. Notice that the failsafe timer applies *only* to Multibus (off-board) requests. If you want the failsafe timer to *interrupt* processing when asserted, refer to Section 2-15 (EDGE INTR paragraph) for additional information.

2-23. iSBX™ MULTIMODULE BOARD MODE SELECTION

The iSBC 86/05 board will support both 8-bit and 16-bit iSBX Multimodule expansion boards. There is a jumper connection for each iSBX connector, which specifies whether it is an 8-bit board or a 16-bit board. The jumper connections are as follows:

iSBX Connector	Jumpers	8-Bit	16-Bit
J3	208 - 209	OUT*	IN
J4	206 - 207	OUT*	IN

Note: * indicates factory default connection.

2-24. MULTIBUS™ INTERFACE ARBITRATION

The 8289 Bus Arbiter operates in conjunction with the 8288 Bus controller to interface the 8086 processor to the Multibus interface. The 8289 Bus Arbiter can operate in several modes, depending on how it is jumper wired and the status of Common Bus Request (CBRQ/).

Common Bus Request. Common Bus Request (CBRQ/), a bidirectional Multibus interface signal, allows a bus master to retain control of the system bus without contending for it each transfer cycle, as long as no other master is requesting control of the bus. A bus master requesting control of the bus, but not currently controlling it, asserts CBRQ/. This causes the controlling bus master to relinquish control of the bus when the proper surrender conditions exist. (See Table 2-14 for surrender conditions.)

The CBRQ/ pins of all the bus master devices that support CBRQ/ are connected together on the iSBC 604/614 modular backplane. When a bus master needs a bus resource, it informs the other bus masters that it is requesting the bus by activating CBRQ/, BREQ/, and/or BPRO/. When the controlling master releases the bus, the bus exchange operates the same as described in paragraph 4-14.

Table 2-13. Wait State Generator Jumpers & Times

Function	Jumper Connection	Number of Waits	8 MHz Time**	5 MHz Time**
PROM Wait	6 - 5	0	282	517
	6 - 4	1	407	717
	6 - 7*	2	532	917
	6 - 8	3	657	1117
I/O Wait	1 - 2	1	372	597
	2 - 3*	2	497	797
INT ACK Wait	9 - 10	2	497	797
	10 - 11*	3	622	997

Notes: * indicates factory default connection.
** indicates all times specified in nanoseconds; Address to Data.

CBRQ/ improves bus access time by allowing a bus master to retain control without contending for it each transfer cycle, as long as no other master is requesting control of the bus.

There are typically two priority resolution schemes used on the system bus: Serial and parallel. When common bus request is used, it operates identically in parallel and serial priority resolution schemes.

Any Request. The 8289 Bus Arbiter has a jumper option (ANYRQST) that controls, in conjunction with BPRN/ and CBRQ/, under what conditions the Multibus interface will be surrendered. The following paragraphs describe this option.

When ANYRQST is jumpered to a low level (189 - 190), the bus arbiter that was in control of the Multibus interface will retain control unless one of the following conditions exist.

1. A higher priority bus master requests the Multibus interface (as indicated by the BPRN/ signal going high).
2. The next transfer cycle of the iSBC 86/05 board does not require the use of the Multibus interface, and CBRQ/ is low.

When ANYRQST is jumpered to a high level (188 - 189), it permits the Multibus interface to be surrendered to a higher or lower priority bus master as though it were a bus master of high priority. A lower priority master indicates it is requesting the Multibus interface by activating CBRQ/. When this option is used, the bus master that is in control will surrender the bus as soon as possible.

If the CBRQ/ pin on the 8289 Bus Arbiter is jumpered to ground (184 - 185) removing it from the Multibus interface, and ANYRQST is jumpered to a high level (188 - 189), the Multibus interface is surrendered after each transfer cycle.

2-25. DUAL PORT RAM LOCK

This signal originates from the iSBC 86/05 board, and is used to prevent access to any system level dual port RAM. To use this feature, install a jumper between posts 214 - 215. The lock signal (LOCK/) is generated when a locked Multibus access (either by OVERRIDE or PROCESSOR LOCK) is requested. It exits the board on Multibus pin P1-25.

Table 2-14. 8289 Bus Arbiter Jumper Configurations

Configuration Number	Jumper Conn	CBRQ/	ANYRQST	Description
1		Low	Low	The Bus Arbiter that has control of the Multibus interface will retain control unless a higher priority master activates CBRQ/ or if the next machine cycle does not require the use of the Multibus interface it will be relinquished to a lower priority device.
	183 - 184 189 - 190	High	Low	The Bus Arbiter that has control of the Multibus interface, retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
2		Low	High	The Bus Arbiter that has control of the Multibus interface will surrender control to the Bus Arbiter that is pulling CBRQ/ low, regardless of its priority, upon completion of the current bus cycle.
	188 - 189* 183 - 184*	High	High	The Bus Arbiter that has control of the Multibus interface, retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
3	184 - 185 188 - 189	Low	High	The Bus Arbiter that has control of the Multibus interface will surrender the use of the Multibus interface after each transfer cycle.

*Factory default wiring.

2-26. BOARD PRIORITY RESOLUTION

Your iSBC 86/05 board has been designed as a "full master" board. This means the board is equipped with bus arbitration logic and can acquire and relinquish control of the common system Multibus lines (see Section 4-14). In order for this system to be effective, a board priority scheme should be established in your system.

If your iSBC 86/05 board is the only master in the system, you must place it in the top cardcage slot (slot J2) or in a slot which has BPRN/ grounded. Normally, pin 15 (BPRN/) of the iSBC 604 backplane is grounded with a jumper between wirewrap posts B and N. (However, this connection should be verified if the factory configuration has been modified.) In this configuration, the remaining three slots can be used for any expansion boards or for lower priority master boards.

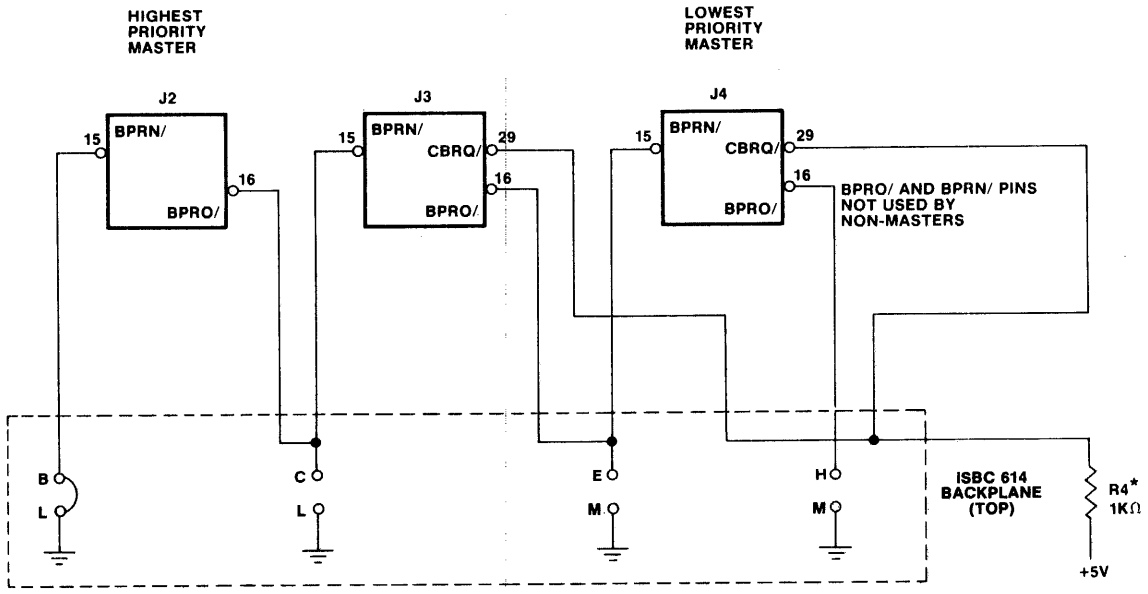
If your system includes more than one master board (CPU board), you must establish a board priority scheme. There are two methods of priority resolution available: Serial and parallel. These are described in Sections 2-21 and 2-22.

Another important consideration in setting up a multimaster system is the Multibus clock signal source. You must ensure only one of the master boards is supplying the BCLK/ and CCLK/ signals to the Multibus lines. All master boards have provisions for disabling the output of these two signals (i.e., preventing the signals from going off-board). The iSBC 86/05 board BCLK/ and CCLK/ signals can be disabled by removing to jumper connections. Refer to Section 2-11 for this information.

2-27. SERIAL PRIORITY RESOLUTION

Serial priority is implemented by board placement. If your iSBC 86/05 board resides in slot J2, as previously described, the next lower priority will be assigned to slot J3. Slot J4 will have the lowest priority in this scheme. Due to the propagation delay of the BPRO/ signal path, this scheme is limited to a maximum of three master boards. In the configuration shown in Figure 2-5, the master board installed in slot J2 has the highest priority and is able to acquire control of the Multibus lines anytime the bus is not busy. This is because the BPRN/ input is always true (tied to ground via jumper connection B - N on the backplane).

If the master board in slot J2 desires control of the Multibus lines, it drives its BPRO/ output high (false) and inhibits the BPRN/ inputs to the remaining lower priority master boards. The master board then takes control of the Multibus lines when the

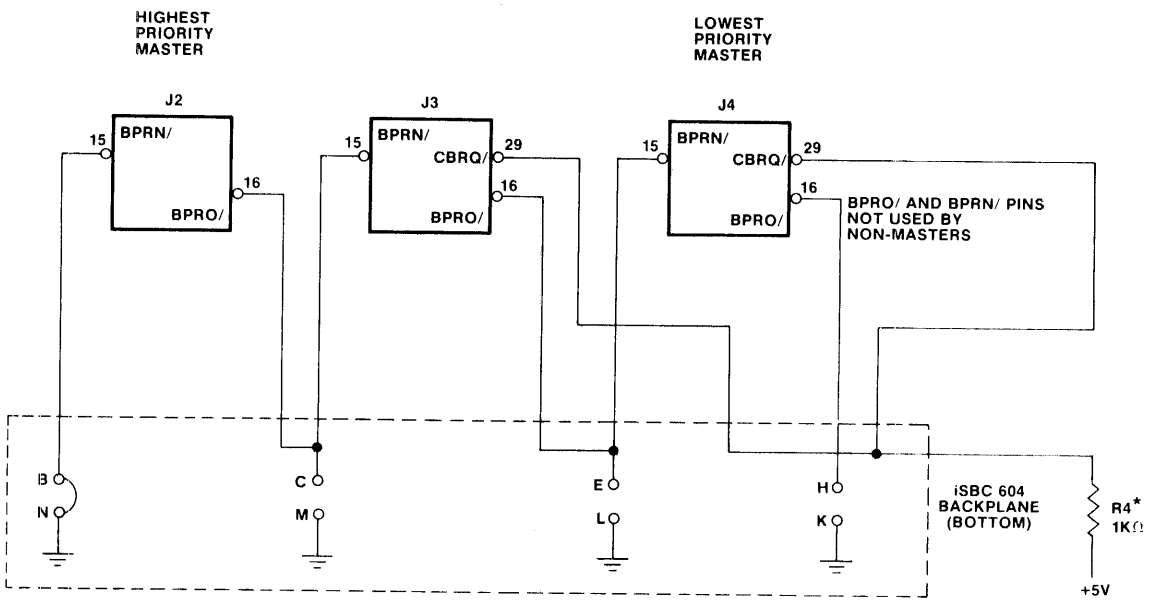


*Pull-up resistor is supplied by the customer.

NOTE: All non CBRQ/ devices must have higher priority. If a non CBRQ/ device is placed at a lower priority, it will not be able to gain control of the Multibus interface.

Top Backplane In Stacked System

Figure 2-5. Serial Priority Resolution Scheme



*Pull-up resistor is supplied by the customer.

NOTE: All non CBRQ/ devices must have higher priority. If a non CBRQ/ device is placed at a lower priority, it will not be able to gain control of the Multibus interface.

Single Backplane In Non-Stacked System

Figure 2-5. Serial Priority Resolution Scheme (Continued)

current bus cycle is completed. When finished using the Multibus lines, the J2 master board pulls its BPRO/ output low (true) and gives the J3 master board the opportunity to acquire Multibus line control. If the J3 master board does not want the Multibus lines, it pulls its BPRO/ output low (true) and gives the J4 master board the opportunity to assume control of the Multibus lines.

Stacked Chassis

If your system uses multiple stacked chassis, the jumper between posts B and N should be removed and placed between posts B and L on the top slot of the uppermost expansion backplane. This will ground BPRN/ as described above. Install the highest priority master in the uppermost slot.

2-28. PARALLEL PRIORITY RESOLUTION

A parallel priority resolution scheme allows up to 16 bus masters in a single system to acquire and control the Multibus lines. Figure 2-6 illustrates one method of implementing such a scheme for resolving bus contention in a system using eight bus masters. Notice that the two highest and two lowest priority bus masters are shown installed in the master chassis. The other masters in this example are installed in the expansion chassis.

In the scheme shown in Figure 2-6, the priority encoder is a Texas Instruments 74148 device, and the priority decoder is an Intel 8205 device. Input connections to the priority encoder determine the bus priority, with input 7 having the highest priority and input 0 having the lowest priority. In Figure 2-6, the master board in J3 has the highest priority and the master board in J5 has the lowest priority.

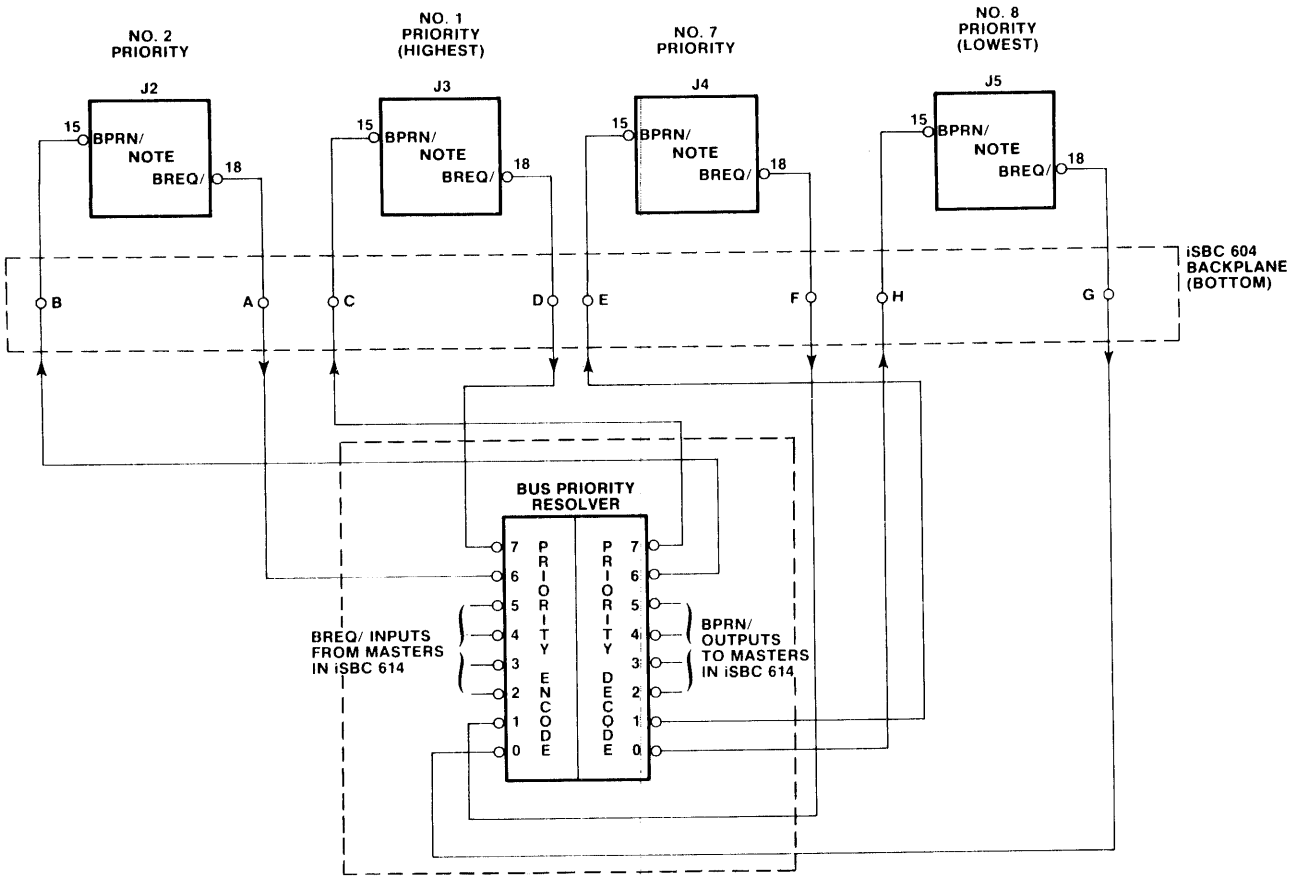
NOTE

In a parallel priority resolution scheme, the BPRO/ output must be disabled on all master boards. Refer to the appropriate hardware reference manual for instructions.

2-29. CONNECTOR INFORMATION

For system applications the iSBC 86/05 board is designed for installation into a standard Intel Multibus cardcage assembly such as the iSBC 604 Cardcage or the iSBC 614 Expansion Cardcage. For OEM applications the board may be interfaced to other hardware by means of separately purchased Multibus compatible connectors. Table 2-14A lists recommended suppliers for such connectors.

Parallel and serial I/O connector information is also supplied in Table 2-14. For related information on parallel I/O and serial I/O cabling, refer to Sections 2-23 and 2-24.



*Note: The user must implement logic, wire to mother board, and provide mounting.

Figure 2-6. Parallel Priority Resolution Scheme

2-30. MULTIBUS™ SIGNAL CHARACTERISTICS

Multibus connector P1 and auxiliary connector P2 interface the iSBC 86/05 board signals and power lines to the other boards in your system and the power supply. Where applicable, these signals conform to the Intel Multibus Interface standard. Pin assignments for P1 and P2 are listed in Tables 2-15 and 2-17 respectively. Signal definitions are provided in Table 2-16 and 2-18.

DC characteristics of the P1 signals used on the iSBC 86/05 board are provided in Table 2-19. P2 signal characteristics are listed in Table 2-20.

The signal names indicate whether or not the signal lines on the MULTIBUS are active high or active low. If the signal name ends with a slash ("/"), then the logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	H = TTL high state	5.25V≥H≥2.0V	5.25V≥H≥2.4V
1	L = TTL low state	.8V≥L≥-.5V	.5V≥L≥0V

If the signal name has no slash (no "/"), then the logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	L = TTL low state	.8V≥L≥.5V	.5V≥L≥0V
1	H = TTL high state	5.25V≥H≥2.0V	5.25V≥H≥2.4V

These specifications are based on TTL where the power source is 5 volts ± 5%, referenced to logic ground (GND).

Table 2-14A. User Furnished Connector Details

Function	# of Pins	Centers (Inches)	Connector Type	Vendor	Vendor Part No.	Intel Part No.
Parallel I/O Connector J1	25/50	0.1000	Flat Crimp	3M 3M AMP ANSLEY SAE	3415-0001 W/ears 3415-0000 W/ears 88083-1 609-5015 S06750 Series	102211-003 N/A
			Soldered Pierced tail	GTE SYLVANIA MASTERITE MICRO PLASTICS VIKING	6AD01-25-1A1-DD NDD8GR25-DR-H-X MP-0100-25-DP-1 3KH25/9JN5	102237-001
			Wire Wrap	VIKING TI ITT CANNON	3KH25/JND5 H421011-25 EC4A050A1A	N/A
Serial I/O Connector J2	13/26	0.100	PCB Soldered Mounting Holes	AMP EDAC	1-583715-1 345-026-520-202	102233-001
			Flat Crimp	3M AMP	3462-0001 88373-5	102210-001
			Soldered Pierced Tail	EDAC	345-026-500-201	N/A
			Wire Wrap	EDAC	345-026-540-201	N/A
iSBX Multi-Module Connector J3/J4	44 36	0.100 0.100	Soldered PCB Soldered PCB	VIKING VIKING	293-001 292-001	iSBC 961-5 iSBC 960-5
Multibus Connector (P1)	43/86	0.156	Soldered PCB Mount	ELFAB VIKING	BS1562043PBB 2KH43/9AMK12	102247-001
			Wire Wrap No Ears	EDAC ELFAB	337-086-0540-201 BW1562D43PBB	102248-001
			Wire Wrap With .128 Dia. Mounting Holes	EDAC ELFAB	337-086-540-202 BW1562A43PBB	102273-001
Auxiliary Connector (P2)	30/60	0.100	Wire Wrap	EDAC ELFAB	345-060-524-802 BS1020A30PBB	102238-001
			With .128 Dia. Mounting Holes	TI VIKING	H421121-30 3KH30/9JNK	
			Wire Wrap No Ear	EDAC ELFAB	345-060-540-201 BW1020D30PBB	102241-001

NOTES:
1. Connector heights are not guaranteed to conform to OEM packaging equipment.
2. Wirewrap pin lengths are not guaranteed to conform to OEM packaging equipment.
3. Connector numbering convention may not agree with board connector numbers.

Table 2-15. Multibus™ Interface Connector P1 Pin Assignments.

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN[1]	MNEMONIC	DESCRIPTION	PIN[1]	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9	-5V	-5Vdc	10	-5V	-5Vdc
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Priority In	16	BPRO/	Bus Priority Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit RAM[2]
BUS CONTROLS AND ADDRESS	25	LOCK/	Dual Port Lock	26	INH2/	Inhibit ROM[2]
	27	BHEN/	Byte High Enable	28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33	INTA/	Interrupt Acknowledge	34	AD13/	
INTERRUPTS	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/		64	DATB/	
	65	DAT8/	Data	66	DAT9/	Data
	67	DAT6/	Bus	68	DAT7/	Bus
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77	—	Reserved	78	—	Reserved
	79	-12V	-12Vdc	80	-12V	-12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

1. All odd-numbered pins (1, 3, 5 . . . 85) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top. All unassigned pins are reserved.
2. Not Used on the iSBC 86/05 board.

Table 2-16. Connector P2 Pin Assignments

Pin Assignment	Signal Mnemonic	Description
P2-1, 2 P2-21, 22	Signal GND	Battery Ground
P2-3 P2-4	+5V AUX	Battery +5V Power Input
P2-6	Reserved	Reserved
P2-17	PFSN/	Power Fail Sense
P2-19	PFIN/	Power Fail Interrupt
P2-20	MPRO/	Memory Protect
P2-31	PLC	Power Line Clock
P2-32	ALE	Bus Master ALE
P2-36	BD RESET/	Board Only Reset
P2-38	AUX RESET/	System Reset Switch Input

Table 2-17. Multibus™ Interface Signal Functions

Signal	Functional Description
ADR0/-ADRF/ ADR10/-ADR13/	*Address.* These 20 lines transmit the address of the memory location or I/O port to be accessed. For memory access, ADR0/ (when active low) enables the even byte (DAT0/-DAT7/) on the Multibus interface; i.e., ADR0/ is active low for all even addresses. ADR13/ is the most significant address ibt.
BCLK/	*Bus Clock.* Used to synchronize the bus contention logic on all bus masters. When generated by the iSBC 86/12A board, BCLK/ has a period of 108.5 nanoseconds (9.22 MHz) with a 35-65 percent duty cycle.
BHEN/	*Byte High Enable.* When active low, enables the odd byte (DAT8/-DATF/) onto the Multibus interface.
BPRN/	*Bus Priority In.* Indicates to a particular bus master that no higher priority bus master is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPRO/	*Bus Priority Out.* In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	*Bus Request.* In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	*Bus Busy.* Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	*Common Bus Request.* Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller raises the CBRQ/ signal.
CCLK/	*Constant Clock.* Provides a clock signal of constand frequency for use by other system modules. When generated by the iSBC 86/12A board, CCLK/ has a period of 108.5 nanoseconds (9.22 MHz) with a 35-65 percent duty cycle.
DAT0/-DATF/	*Data.* These 16 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DATF/ is the most-significant bit. For data word operations, DAT0-DAT7/ is the even byte and DAT8/-DATF/ is the odd byte.
LOCK	*Dual Port RAM Lock.* Disables system dual Port RAM when asserted and jumper is installed See section 2-25.

Table 2-17. Multibus™ Interface Signal Functions (Continued)

Signal	Functional Description
INIT/	*Initialize.* Resets the entire system to a known internal state.
INTA/	*Interrupt Acknowledge.* This signal is issued in response to an interrupt request.
INT0/-INT7/	*Interrupt Request.* These eight lines transmit Interrupt Requests to the appropriate interrupt handler. INT0 has the highest priority.
IORC/	*I/O Read Command.* Indicates that the address of an I/O port is on the Multibus interface address lines and that the output of that port is to be read (placed) onto the Multibus interface data lines.
IOWC/	*I/O Write Command.* Indicates that the address of an I/O port is on the Multibus interface interface address lines and that the contents on the Multibus interface data lines are to be accepted by the addressed port.
MRDC/	*Memory Read Command.* Indicates that the address of a memory location is on the Multibus interface address lines and that the contents of that location are to be read (placed) on the Multibus interface data lines.
MWTC/	*Memory Write Command.* Indicates that the address of a memory location is on the Multibus interface address lines and that the contents on the Multibus interface data lines are to be written into that location.
XACK/	*Transfer Acknowledge.* Indictes that the addressed memory location has completed the specified read or write operation. That is, data has been placed onto or accepted from the Multibus interface data lines.

Table 2-18. P2 Signal Definitions

PFIN/	*Power Fail Interrupt.* This input from the power supply interrupts the CPU when a power failure occurs. See section 2-33.
PFSN/	*Power Fail Sense.* This line is the output of a latch which indicates a power failure has occurred. It is reset by PFSR/ and must be powered by the standby power source. See section 2-33.
MPRO/	*Memory Protect.* When true, this externally generated signal prevents access to the on-board RAM during periods of uncertain DC power. See section 2-33.
ALE	*Address Latch Enable.* Indicates the 8086 CPU is operating. Typically, this signal is used to drive a front panel RUN indicator.
BD RESET/	*Board Reset.* This signal resets the iSBC 86/05 board only. It will not reset other boards in the system.
AUX RESET/	*Auxiliary Reset.* Typically this RESET signal is generated by a front panel switch. The signal is functionally equivalent to INIT/.

Table 2-19. iSBC 86/05™ Board DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
AACK/, XACK/	V_{OL}	Output Low Voltage	I_{OL}= 16 mA		.04	V
	V_{OH}	Output High Voltage	I_{OH} = -3 mA	2.0		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-2.2	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		-1.4	mA
	*C_L	Capacitive Load			15	pF
ADR0/-ADRF/ ADR10/-ADR13/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.55	V
	V_{OH}	Output High Voltage	I_{OH} = 3 mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.50	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		50	μA
	I_{LH}	Output Leakage High	V_O = 5.25V		-0.50	mA
	I_{LL}	Output Leakage Low	V_O = 0.45V		-0.50	mA
	*C_L	Capacitive Load			18	pF
BCLK/	V_{OL}	Output Low Voltage	I_{OL} = 59.5 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -3 mA	2.7		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		40	μA
	*C_L	Capacitive Load			15	pF
BHEN/	V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
	V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		1.6	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		40	μA
	*C_L	Capacitive Load			15	pF
BPRN/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		50	μA
	*C_L	Capacitive Load			18	pF
BPRO/	V_{OL}	Output Low Voltage	I_{OL} = 5.0 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -0.4 mA	2.4		V
	*C_L	Capacitive Load			15	pF
BREQ/	V_{OL}	Output Low Voltage	I_{OL} = 50 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -0.4 mA	2.4		V
	*C_L	Capacitive Load			10	pF
BUSY/, CBRQ/, INTROUT/ (OPEN COLLECTOR)	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		0.45	V
	V_{IL}	Input Low Voltage			0.4	V
	V_{IH}	Input High Voltage		2.4		V
	I_{IL}	Input Current at Low V	V_{IN}= 0.45V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		40	μA
	*C_L	Capacitive Load			20	pF

Table 2-19. iSBC 86/05™ Board DC Characteristics (Continued)

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
CCLK/	V_{OL}	Output Low Voltage	I_{OL} = 60 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -3 mA	2.7		V
	*C_L	Capacitive Load			15	pF
DAT0/-DATF/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.80	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.20	mA
	I_{LH}	Output Leakage High	V_O = 5.25V		100	μA
	*C_L	Capacitive Load			18	pF
LOCK/	**V_{OL}**	**Output Low Voltage**	**I_{OL} = 32**		0.8	V
	V_{OH}	**Output High Voltage**	**I_{OH} = -2**	2.0		V
	*C_L	Capacitive Load			**300**	pF
INIT/ (SYSTEM RESET)	V_{OL}	Output Low Voltage	I_{OL} 44 mA		0.4	V
	V_{OH}	Output High Voltage	OPEN COLLECTOR			
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} 0.4V		-4.2	mA
	I_{IH}	Input Current at High V	V_{IN} 2.4V		-1.4	mA
	*C_L	Capacitive Load			15	pF
INT0/-INT7/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} 0.4V		-1.6	mA
	I_{IH}	Input Current at High V	V_{IN} 2.4V		40	μA
	*C_L	Capacitive Load			18	pF
IORC/, IOWC/	V_{OL}	Output Low Voltage	I_{OL} 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} -5 mA	2.4		V
	I_{LH}	Output Leakage High	V_O 5.25V		100	μA
	I_{LL}	Output Leakage Low	V_O 0.45V		-100	μA
	*C_L	Capacitive Load			15	pF
INTA/, MRDC/, MWTC/	V_{OL}	Output Low Voltage	I_{OL} 30 mA		0.45	V
	V_{OL}	Output High Voltage	I_{OH} -5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-2.0	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25		1000	μA
	*C_L	Capacitive Load			25	pF

*Capacitive load values are approximations.

Table 2-20. Auxiliary Signal (Connector P2) DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
ALE	V_{OL}	Output Low Voltage	I_{OL} = 8 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	2.4		V
	*C_L	Capacitive Load			20	pF
PFIN/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.4		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-0.4	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		20	μ
	*C_L	Capacitive Load			20	pF
MPRO/	V_{IL}	Input Low Voltage			0.80	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-6.0	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		250	μA
	*C_L	Capacitive Load			15	pF
AUX RESET/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.6		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.25	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		10	μA
	*C_L	Capacitive Load			10	μF

*Capacitance load values are approximations.

2-31. PARALLEL I/O DC CHARACTERISTICS

Parallel I/O DC characteristics of the iSBC 86/05 board are provided in Table 2-21.

2-32. AC CHARACTERISTICS

AC characteristics of the iSBC 86/05 board are provided in Table 2-22. Refer to the board timing diagram (Figure 2-7) for parameter identification.

2-33. POWER FAIL BATTERY BACKUP PROVISIONS

In an optional mode, the iSBC 86/05 board may be configured for battery backup operation. This means you may have a DC battery connected to the board, which is used to preserve memory during an AC power failure. In order for the battery backup scheme to function, your power supply must provide the following signals:

a. PFIN/ *Power Fail Interrupt.* Asserted at least 8 milliseconds before DC voltages are lost.

b. MPRO/ *Memory Protect.* Asserted at least 50 microseconds before DC voltages are lost.

c. PFSN/ *Power Fail Sense.* The output of an external, battery powered latch which indicates a power failure has occured.

To implement a typical battery backup scheme on the iSBC 86/05 board, the following connections are required:

a. Connect +5 Volt battery positive leads to auxiliary connector pins P2-3 and P2-4.

b. Connect battery return leads to auxiliary connector pins P2-1 and P2-2.

c. Remove jumper connection 177 - 178.

d. Connect power supply PFIN/ line to auxiliary connector P2-19.

e. Remove interrupt jumper 120 - 121 and install jumper 118 - 120. This routes the PFIN/ input to the 8086 NMI input.

Table 2-21. Parallel I/O DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
Port C8 Bidirectional Drivers	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-5.25	mA
	*C_L	Capacitive Load			18	pF
8255A Driver/Receiver	V_{OL}	Output Low Voltage	I_{OL} = 1.7 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -200 μA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45		10	μA
	I_{IH}	Input Current at High V	V_{IN} = 5.0		10	μA
	*C_L	Capacitive Load			18	pF
EXT INTR0/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-1.0	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		-0.8	mA
	*C_L	Capacitive Load			30	pF

*Capacitive load values are approximations.

Table 2-22. AC Characteristics

Parameter	Description	Minimum	Maximum	Units
t_{BCY}	Bus Clock Period	100	D.C.	ns
t_{BW}	Bus Clock Width	0.35 t_{BCY}	0.65 t_{BCY} (not restricted)	
t_{SKEW}	BCLK/skew		3	ns
t_{PD}	Standard Bus Propagation Delay		3	
t_{AS}	Address Set-Up Time (at Slave Board)	50		ns
t_{DS}	Write Data Set Up Time	50		ns
t_{AH}	Address Hold Time	50		ns
t_{DHW}	Write Data Hold Time	50		ns
t_{DXL}	Read Data Set Up Time To XACK	0		ns
t_{DHR}	Read Data Hold Time	0	65	ns
t_{XAH}	Acknowledge Hold Time	0	65	ns
t_{XACK}	Acknowledge Time	0	8	μs
t_{CMD}	Command Pulse Width	100	9.5	μs
t_{INTA}	INTA/ Width	250		ns
t_{CSEP}	Command Separation	100		ns
t_{BREQL}	↑BCLK/ to BREQ/ Low Delay	0	35	ns
t_{BREQH}	↓BCLK/ to BREQ/ High Delay	0	35	ns

Table 2-22. AC Characteristics (Continued)

Parameter	Description	Minimum	Maximum	Units
t_{BPRNS}	BPRN/ to ↓BCLK/ Setup Time	22		ns
t_{BUSY}	BUSY/ delay from ↓BCLK/	0	70	ns
t_{BUSYS}	BUSY/ to ↓BCLK/ Setup Time	25		ns
t_{BPRO}	↓BCLK/ to BPRO/ (CLK to Priority Out)	0	40	ns
t_{BPRNO}	BPRN/ to BPRO/ (Priority In to Out)	0	30	ns
t_{CBRO}	↓BCLK/ to CBRQ/ (CLK to Common Bus Request)	0	60	ns
t_{CBRQS}	CBRQ/ to ↓BCLK/ Setup Time	35		ns
t_{XCD}	XACK↓ to Command Delay	0	1500	ns
t_{BSYO}	CBRQ/↓ and BUSY/↓ to BUSY/↑	—	12	μs
t_{CCY}	C-clock Period	100	110	ns
t_{CW}	C-clock Width	0.35 t_{CCY}	0.65 t_{CCY}	ns
t_{INIT}	INIT/Width	5		ms
t_{INITS}	INIT/ to MPRO/ Setup Time	100		ns
t_{PBD}	Power Backup Logic Delay	0	200	ns
t_{PFINW}	PFIN/ Width	2.5		ms
t_{MPRO}	MPRO/ Delay	2.0	2.5	ms

f. Install a jumper between parallel port matrix post 26 and the desired port CC output bit.

g. Connect power supply MPRO/ line to auxiliary connector P2-20.

h. Connect the PFSN/ line to auxiliary connector P2-17. PFSN/ is the output of an external, battery powered latch which indicates that a power failure has occurred. This latch is reset by PFSR/, which can be implemented with an unused port CC bit.

In this typical battery backup configuration, if a power failure occurs, the power supply asserts PFIN/ which in turn initiates the NMI interrupt, placing the board in an idle mode. Contents of various internal registers are stored in RAM, which is then locked up when MPRO/ is asserted. When power is restored, the PFSN/ signal is read by the parallel port, indicating a power failure has occurred. Your power on routine could then read contents of RAM before executing, thereby minimizing data loss.

2-34. PARALLEL I/O CABLING

Parallel I/O C8, CA, and CC are controlled by the 8255A-5 Parallel Peripheral Interface (PPI) device in socket U22, and are connected to external equipment via edge connector J1. Pin assignments for edge connector J1 are provided in Table 2-23. Bit order for port CC may be altered by jumper connection. Refer to Section 2-13 for instructions.

DC characteristics of the parallel I/O port lines are listed in Table 2-21. Connector information for edge connector J1 is provided in Table 2-14.

For maximum reliability, the transmission path from the I/O source to the iSBC 86/05 board should be limited to a maximum of 3 meters (10 feet). Recommended bulk cable types are provided in Table 2-24.

2-35. SERIAL I/O CABLING

Pin assignments and signal names for the serial I/O port interface connector (J2) are listed in Table 2-25. An Intel iSBC 955 Cable Set is recommended for RS 232C interfacing. One cable assembly consists of a 25 conductor flat cable with a 26-pin connector at one end and an RS 232C interface connector at the other end. A second cable assembly is included in the iSBC 955 set, which consists of an RS 232C connector on one end and spade lugs on the other end. The spade lugs are used to connect the cable to a teletypewriter. (Refer to Appendix B for ASR-33 TTY interface instructions.)

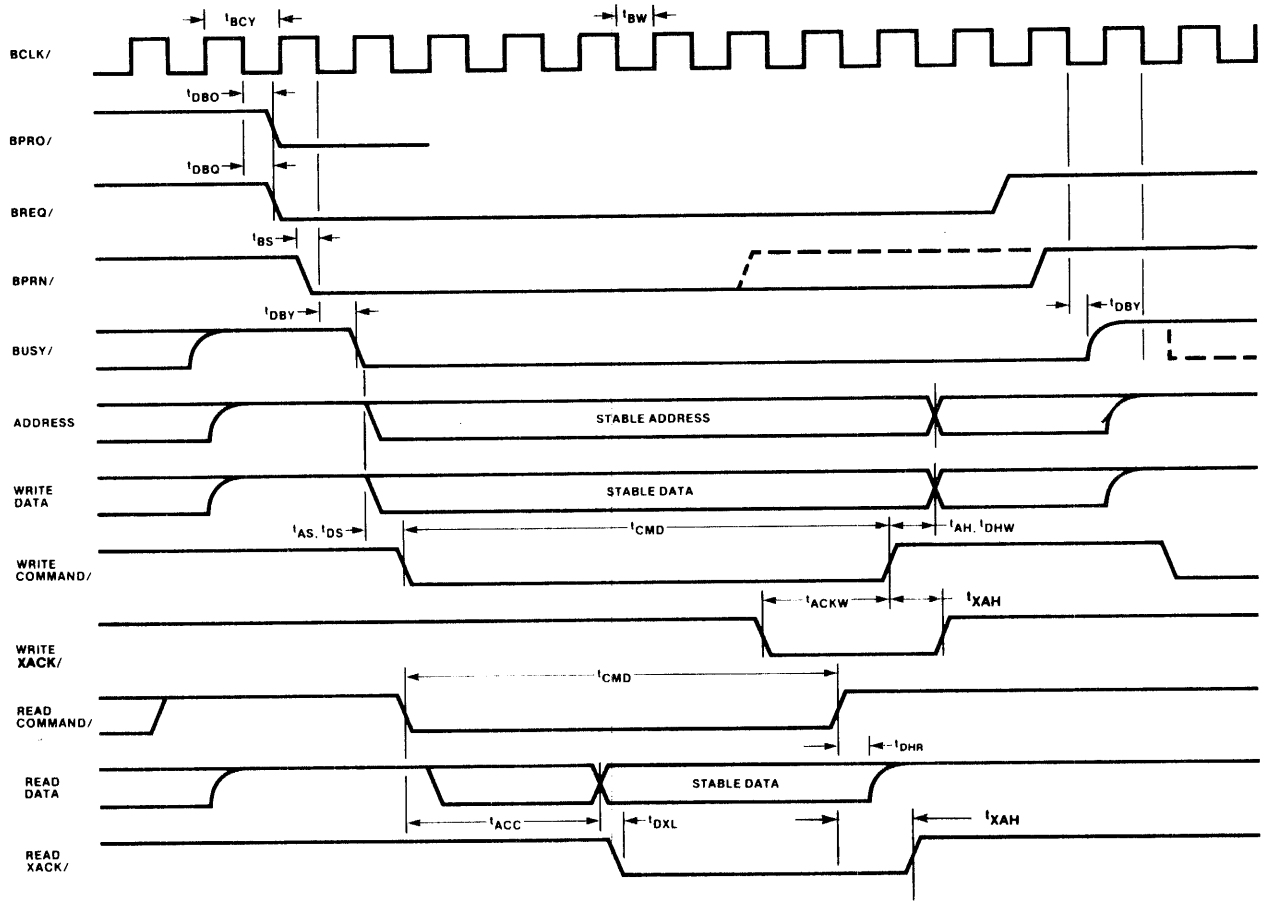


Figure 2-7. Master AC Timing

For OEM applications where cables will be made for the iSBC 86/05 board, it is important to note that the mating connector for J2 has 26 pins, whereas the RS 232C connector has 25 pins. Consequently, when connecting the 26-pin mating connector to 25-conductor flat cable, be sure that the cable makes contact with pins 1 and 2 of the mating connector and not pin 26. Table 2-26 provides pin correspondence between connector J2 and the RS 232C connector. When attaching the connector to J2 be sure that the PC connector is oriented properly with respect to pin 1 on the board. Refer to the footnote at the bottom of Table 2-25.

If your application requires a 20 mA current loop (TTY) interface refer to Section 2-35 and Appendix B.

2-36. CURRENT LOOP (TTY) INTERFACE

To adapt your iSBC 86/05 board to a 20 mA current loop (TTY) interface, optional jumper connections are required. In addition, the iSBC 530 Teletypewriter Adapter module must be installed between the board and the serial peripheral.

CAUTION

Current limiting is not provided for these outputs. If improperly connected, damage to the board and power supply could result.

The optional TTY interface module (iSBC 530 Teletypewriter Adapter) converts iSBC 86/05 board RS 232C signal levels to an optically isolated 20 mA current loop interface. The adapter also provides signal translation for transmitted data, received data and a teletypewriter paper tape reader relay. Installation instructions for the adapter are provided in Appendix B.

Table 2-23. Parallel I/O Connector J1 Pin Assignments

Pin[1,2]	Function	Pin[1,2]	Function
1	Ground	2	Port CA bit 7
3		4	Port CA bit 6
5		6	Port CA bit 5
7		8	Port CA bit 4
9		10	Port CA bit 3
11		12	Port CA bit 2
13		14	Port CA bit 1
15	Ground	16	Port CA bit 0
17	Ground	18	Port CC bit 3
19		20	Port CC bit 2
21		22	Port CC bit 1
23		24	Port CC bit 0
25		26	Port CC bit 4
27		28	Port CC bit 5
29		30	Port CC bit 6
31	Ground	32	Port CC bit 7
33	Ground	34	Port C8 bit 7
35		36	Port C8 bit 6
37		38	Port C8 bit 5
39		40	Port C8 bit 4
41		42	Port C8 bit 3
43		44	Port C8 bit 2
45		46	Port C8 bit 1
47	Ground	48	Port C8 bit 0
49	Ground	50	EXT INTR0/

1. All odd-numbered pins 1, 3, 5, ... 49) are on component side of board. Pin 1 is the right-most pin when viewed from the component side of the board with the extractors at the top.
2. Cable connector numbering convention may not agree with board connector numbering convention.

Table 2-24. Bulk Cable Types

Flat cable, 50 conductor w/o ground plane	3M 3306-50
Flat cable, 50 conductor with ground plane	3M 3380-50
Woven cable, 25 pair	3M 3321-25

2-37. MULTIMODULE BOARDS AND THE iSBX BUS

The iSBC 86/05 board is equipped with two iSBX (single board expansion) bus connectors (J3 and J4). This bus allows on-board I/O expansion, using optional iSBX Multimodule boards. These boards should not be confused with the optional RAM and ROM/PROM expansion boards which are interfaced to the on-board memory bus. Connectors J3 and J4 may be used only for iSBX Multimodule boards.

Table 2-25. Connector J2 Pin Assignments

Pin No.	ISBC 86/05 Signal	PCI Function
J2 - 1	Not Used	—
J2 - 2	Protective Ground	Ground
J2 - 3	Not Used	—
J2 - 4	Transmitted Data	RxD Input
J2 - 5	See J2 - 26	See J2 - 26
J2 - 6	Received Data	TxD Output
J2 - 7	External Clock	TxC/RxC Input
J2 - 8	Request To Send	CTS/ Input
J2 - 9	Not Used	—
J2 - 10	Clear To Send	RTS/ Output
J2 - 11	Not Used	—
J2 - 12	Data Set Ready	DSR/ Input
J2 - 13	Data Terminal Ready	DTR/ Output
J2 - 14	Signal Ground	GND
J2 - 15	Not Used	—
J2 - 16	Not Used	—
J2 - 17	Not Used	—
J2 - 18	Not Used	—
J2 - 19	-12 Vdc[3]	—
J2 - 20	Not Used	—
J2 - 21	See J2 - 26[3]	See J2 - 26
J2 - 22	+12 Vdc[3]	—
J2 - 23	+5 Vdc[3]	—
J2 - 24	Not Used	—
J2 - 25	Ground	GND
J2 - 26	Secondary TxD or Clock Out[3]	STxD or TxC/TxD

Notes:
1. Odd numbered pins are on component side of board; even pins on solder side.
2. Cable connector numbering convention may not correspond with J2 numbering.
3. Not connected at factory.

Table 2-26. RS232 Signals Pin Correspondence

PC Conn. J2	RS232C Conn.	PC Conn. J2	RS232C Conn.
1	14	14	7
2	1	15	21
3	15	16	8
4	2	17	22
5	16	18	9
6	3	19	23
7	17	20	10
8	4	21	24
9	18	22	11
10	5	23	25
11	19	24	12
12	6	25	N/C
13	20	26	13

Table 2-27 provides the iSBX bus connector pin assignments, and Table 2-28 provides signal descriptions. Each of the two connectors has identical pin assignments and physical layout.

For installation instructions, refer to the specific iSBX Multimodule board hardware reference manual.

When a Multimodule board is installed, the iSBC 86/05 board's power requirements will increase by the amount specified in the Multimodule board reference manual.

Table 2-27. iSBX™ Bus Connector Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
43	MD8	MDATA B	44	MD9	MDATA 9
41	MDA	MDATA A	42	MDB	MDATA B
39	MDC	MDATA C	40	MDD	MDATA D
37	MDE	MDATA E	38	MDF	MDATA F
35	GND	SIGNAL GROUND	36	+5V	+5 Volts
33	MD0	MDATA BIT 0	34	—	RESERVED
31	MD1	MDATA BIT 1	32	—	RESERVED
29	MD2	MDATA BIT 2	30	OPT0	OPTION 0
27	MD3	MDATA BIT 3	28	OPT1	OPTION 1
25	MD4	MDATA BIT 4	26	—	RESERVED
23	MD5	MDATA BIT 5	24	—	RESERVED
21	MD6	MDATA BIT 6	22	MCS0/	M CHIP SELECT 0
19	MD7	MDATA BIT 7	20	MCS1/	M CHIP SELECT 1
17	GND	SIGNAL GROUND	18	+5V	+5 Volts
15	IORD/	IO READ COMMAND	16	MWAIT/	M WAIT
13	IOWRT/	IO WRITE COMMAND	14	MINTR0	M INTERRUPT 0
11	MA0	M ADDRESS 0	12	MINTR1	M INTERRUPT 1
9	MA1	M ADDRESS 1	10	—	RESERVED
7	MA2	M ADDRESS 2	8	MPST/	M PRESENT
5	MRESET	M RESET	6	MCLK	M CLOCK
3	GND	SIGNAL GROUND	4	+5V	+5 Volts
1	+12V	+12 Volts	2	-12V	-12 Volts

Table 2-28. iSBX™ Bus Signal Descriptions

IORD/	Commands the Multimodule board to perform the read operation.
IOWRT/	Commands the Multimodule board to perform the write operation.
MRESET/	Initializes the Multimodule board to a known internal state.
MCS0/	Chip select. Selects I/O addresses 80-8F on the J3 Multimodule board and addresses A0-AF on the J4 Multimodule board.
MCS1/	Chip select. Selects I/O addresses 90-9F on the J3 Multimodule board and addresses B0-BF on the J4 Multimodule board.
MA0-2	Least three bits of the I/O address. Used in conjunction with the chip select and command lines.
MPST/	Multimodule present indicator. Informs iSBC 86/05 board that a Multimodule board(s) is installed.
MINTR0-1	Interrupt request lines from the Multimodule board to the iSBC 86/05 board interrupt matrix.
MWAIT/	Causes iSBC 86/05 board to execute wait states until Multimodule board is ready to respond.
MCLK/	9.68 MHz Multimodule board timing reference from iSBC 86/05 board.
OPT0-1	Optional use lines. May be used for additional interrupt request lines.
MD0-F	Bidirectional data lines.

2-38. iRMX 86 SYSTEM SOFTWARE

The iSBC 86/05 board is compatible with Intel's iRMX 86 Real Time Multitasking Operating System. For more information about iRMX 86 features and capabilities, contact your local Intel Field Applications Engineer or Sales Office.

2-39. FINAL INSTALLATION

CAUTION

Always turn off the system power supply before installing or removing the iSBC 86/05 board from its system, or before installing or removing any I/O cables. Failure to observe these precautions may result in damage to the board.

In an iSBC Single Board Computer based system, install the iSBC 86/05 board in the cardcage slot which corresponds to your priority scheme or application. Ensure that an auxiliary connector is installed in the cardcage if any of the iSBC 86/05 board P2 signals are used in your system.

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

Several Intel programmable devices reside on the iSBC 86/05 board. This chapter provides programming information for these devices and gives typical examples for most applications. Memory and I/O addressing are provided in table form, for quick reference.

3-2. MEMORY ADDRESSING

The iSBC 86/05 board may accommodate up to 32K bytes of on-board ROM. Four sockets are provided for ROM devices. The amount of on-board ROM may be doubled by adding the optional iSBC 341 ROM Expansion Module (refer to Section 2-7). Table 3-1 provides the addressing for the various ROM configurations possible on the iSBC 86/05 board.

The factory configuration for 2716 devices (2K X 8) indicates an on-board ROM address range from FE000 to FFFFF (hexadecimal). From Table 3-1 you will notice that on-board ROM addressing always ends at the highest possible address (FFFFF), regardless of size. In the maximum configuration, without the iSBC 341 ROM Expansion Module, the address range would be from F8000 to FFFFF.

Table 3-1. On-Board ROM Addresses

Device Type & Size	Address	Total Space
2716 (2K X 8)	FE000 - FFFFF	8K
2732 (4K X 8)	FC000 - FFFFF	16K
2764 (8K X 8)	F8000 - FFFFF	32K
(16K X 8)	F0000 - FFFFF	64K
ROM Addresses With iSBC 341 ROM Module		
2716 (2K X 8)	FC000 - FFFFF	16K
2732 (4K X 8)	F8000 - FFFFF	32K
2764 (8K X 8)	F0000 - FFFFF	64K
(16K X 8)	E0000 - FFFFF	128K
Notes: 1. Device sizes cannot be mixed.		

In the factory configuration 8K bytes of RAM reside on-board. RAM addressing in this configuration is assigned from 0000 to 1FFF (hexadecimal). With the optional iSBC 302 RAM Expansion Module installed, RAM addressing becomes 0000 - 3FFF. Notice that on-board RAM always starts at the lowest possible address (0000). Table 3-2 summarizes on-board RAM addressing.

Table 3-2. On-Board RAM Addresses

Configuration	Addresses	Total Size
Factory Default	0 - 1FFF	8K
With iSBC 302	0 - 3FFF	16K

If non-existent memory is addressed, the on-board failsafe timer will force the CPU to execute wait states for approximately 10 milliseconds. Following this an acknowledge signal will be sent to the CPU, allowing processing to resume. For failsafe timer jumper information, refer to Section 2-11.

When the CPU is addressing on-board memory, an internal PROM or RAM Acknowledge signal is automatically generated to prevent imposing a CPU wait state. When the CPU is addressing off-board system memory via the Multibus lines, the CPU must first gain control of the Multibus lines and, after the Memory Read or Memory Write command is given, it must execute wait states until a Transfer Acknowledge signal is received from the addressed memory.

3-3. I/O ADDRESSING

The on-board 8086 CPU communicates with the programmable devices through a sequence of I/O read and I/O write commands. Each device has a specific fixed (dedicated) address, or group of addresses, through which commands and or data are issued or accepted. All of these fixed on-board I/O addresses are listed in Table 3-3. In addition to the board's programmable I/O devices, certain other functions have specific addresses assigned to them. These addresses are also included in the table.

Table 3-3. I/O Port Addresses

Address	Device	Input Function	Output Function
C0 or C4	8259A PIC	ICW1/OCW2/OCW3	Status & Poll
C2 or C6	8259A PIC	ICW2/ICW3/ICW4/OCW1 Mask	OCW1 Mask
C8	8255A PPI	Port A	Port A
CA	8255A PPI	Port B	Port B
CC	8255A PPI	Port C	Port C
CE	8255A PPI	Control Word	None
D0	8253 PIT	Counter 0	Counter 0
D2	8253 PIT	Counter 1	Counter 1
D4	8253 PIT	Counter 2	Counter 2
D6	8253 PIT	Control Word	None
D8 or DC	8251A PCI	Data	Data
DA or DE	8251A PCI	Mode or Command Word	Status

iSBX™ Multimodule Connector I/O Port Addresses

Addresses	Connector	Mode	Select	Description
A0 A2 A4 A6 A8 AA AC AE	J3	8-bit	MCS0/	SBX 2 CS0/
B0 B2 B4 B6 B8 BA BC BE	J3	8-bit	MCS1/	SBX 2 CS1/
A1 A3 A5 A7 A9 AB AD AF	J3	16-bit	MCS1/	SBX 2 CS1/
80 82 84 86 88 8A 8C 8E	J4	8-bit	MCS0/	SBX 1 CS0/
90 92 94 96 98 9A 9C 9E	J4	8-bit	MCS1/	SBX 1 CS1/
81 83 85 87 89 8B 8D 8F	J4	16-bit	MCS1/	SBX 1 CS1/

3-4. SYSTEM INITIALIZATION

When power is initially applied to the board, the reset signal (RESET) is automatically generated by the 8284A Clock Generator/Driver. This clears the 8086 internal counters, instruction registers, and the interrupt enable circuitry. The first instruction is then executed from memory location FFFF0. This location should contain a JMP instruction which directs the processor to the actual program beginning.

The RESET signal also is routed to all other iSBC boards in your system (as INIT/) via Multibus line P1 - 14. On-board, the RESET signal is routed to the 8255A parallel interface, the 8251A serial interface, the interrupt acknowledge circuitry, and the iSBX connectors. The RESET signal causes:

a. The 8251A serial interface device to idle and wait for a set of command words; and

b. Sets the 8255A parallel ports to mode 0, input.

The reset/initialize signal can also be generated by an auxiliary reset switch, such as on a system front panel. This switch should be connected to P2 - 38 (AUX RESET/) on the auxiliary connector.

Another switch may be used to generate an on-board only RESET. This switch should be connected to P2 - 36 (BD RESET/) on the auxiliary connector.

3-5. 8253 INTERVAL TIMER PROGRAMMING

The on-board 8253 interval timer has three independent counter outputs. Each counter has its own input. Each counter may be programmed to operate in one of six different modes. In addition, the iSBC 86/05 board interval timer configuration provides several jumper selectable clock rates which can be used for counter inputs. Normally, the counter output 2 is used as the baud rate generator for the 8251A serial interface device.

Jumper configurations for the interval timer clock inputs are summarized in Section 2-11. In the default configuration, the following frequencies are jumpered to the interval timer:

1.23 MHz to CLK 0 Input
153.60 KHz to CLK 1 Input
1.23 MHz to CLK 2 Input

Sections 3-6 through 3-9 describe interval timer mode control, addressing, initialization, and operation as implemented on the iSBC 86/05 board.

3-6. MODE CONTROL WORD & COUNT

All three counters must be initialized separately prior to their use. The initialization for each counter consists of two steps:

a. A mode control word (Figure 3-1) is written to the control register for each individual counter.
b. A down-count number is loaded into each counter. One or two bytes must be sent to the PIT, as determined by the mode control word.
c. Load most-significant byte of count into Counter 0 at port D0.

NOTE

Be sure to enter the downcount in two bytes if the counter was programmed for a two-byte entry in the mode control word. Similarly, enter the downcount value in BCD if the counter was so programmed.

d. Repeat steps a, b, and c for Counters 1 and 2.

3-7. OPERATION

The following paragraphs describe operating procedures for a counter read, clock frequency divider/ratio selection, and interrupt timer count selection.

3-8. COUNTER READ. There are two methods that can be used to read the contents of a particular counter. The first method involves a simple read of the desired counter. The only requirement with this method is that, in order to ensure a stable count reading, the desired counter must be *inhibited* by controlling its gate input. Only Counter 0 and Counter 1 can be read using this method because the gate input to Counter 2 is not controllable.

The second method allows the counter to be read "on-the-fly." The recommended procedure is to use a mode control word to latch the contents of the count register; this ensures that the count reading is accurate and stable. The latched value of the count can then be read.

NOTE

If a counter is read during count, it is mandatory to complete the read procedure; that is, if two bytes were programmed to the counter, then two bytes *must* be read before any other operations are performed with that counter.

The mode control word (Figure 3-1) does the following:

a. Selects counter to be loaded.
b. Selects counter operating mode.
c. Selects one of the following four counter read/load functions:
   (1) Counter latch (for stable read operation).
   (2) Read or load most-significant byte only.
   (3) Read or load least-significant byte only.
   (4) Read or load least-significant byte first, then most-significant byte.
d. Sets counter for either binary or BCD count.

Before you can use one or all of the counters, they must be programmed for mode and count. The mode can be programmed at any time with the Mode Control Word (Figure 3-1). This word specifies which counters are selected, what their mode is, and the type of count byte which will subsequently be sent.

Notice that the Read/Load sequence specified by the Mode Control Word with the RL bits (Figure 3-1) *must* be followed when these bytes are sent to the PIT. These bytes do not necessarily have to follow the associated Mode Control Word. For example, if you select RL1=0 and RL0=1, indicating Read/Load *least* significant byte only, your desired count must be placed in the least significant count byte. This is especially important when using counts which require two bytes.

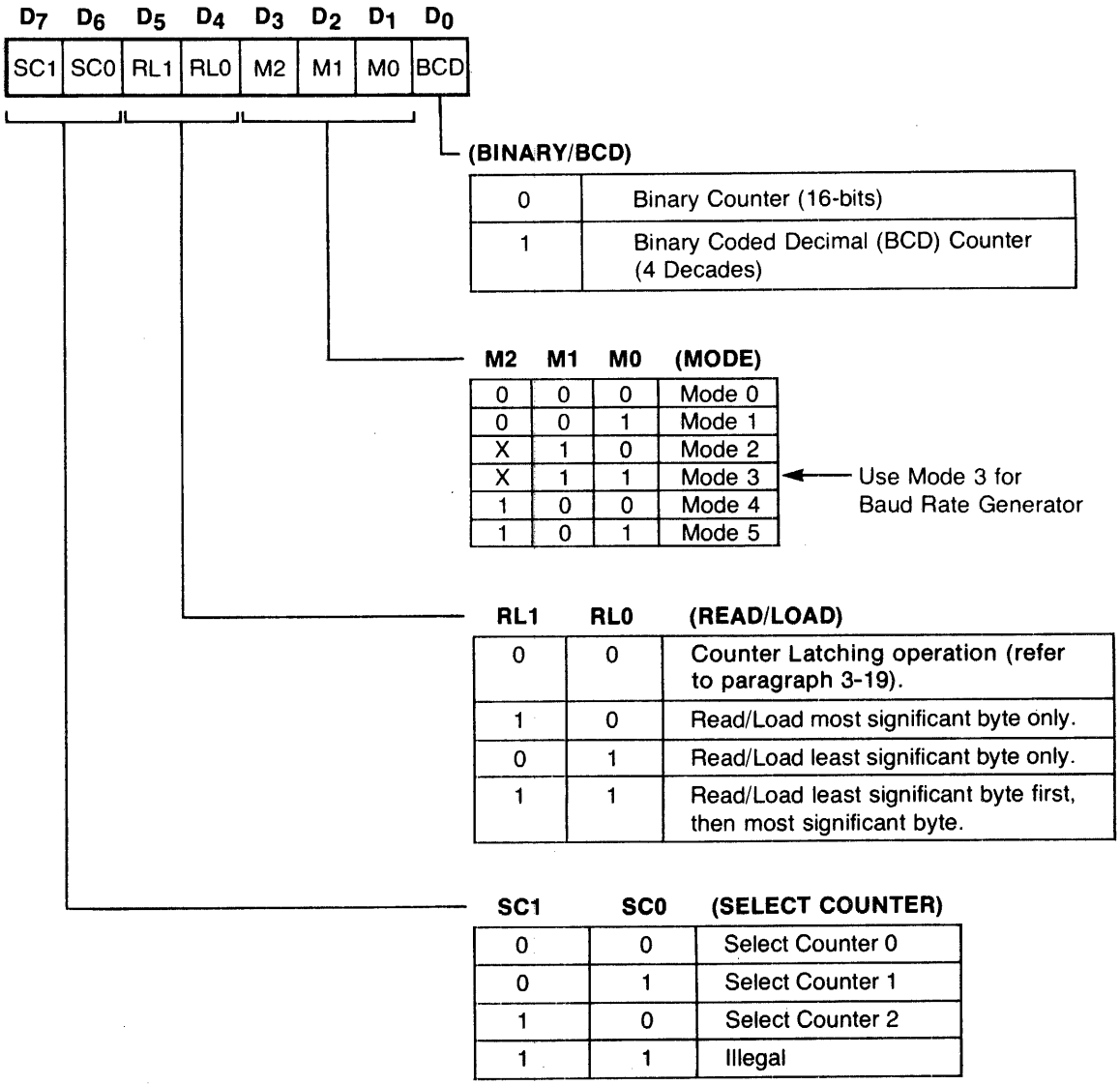


Figure 3-1. PIT Mode Control Word Format

If this procedure is followed for each counter, the PIT can be programmed in any convenient sequence. For example, Mode control words for each counter can be loaded-first followed by the count byte. Figure 3-2 illustrates a typical PIT programming sequence.

Since all PIT counters are downcounters, the values loaded into the count registers are decremented. Loading all zeros into a count register results in the maximum count possible: 2^{16} for binary numbers and 10^4 for BCD numbers.

The count mode selected in the control word controls the counter output. As shown in Figure 3-1, the PIT device can operate in any of six modes:

a. Mode 0: Interrupt on terminal count. In this mode, Counters 1 and 2 can be used for auxiliary functions such as generating real-time interrupt intervals. After the count value is loaded into the count register, the counter output goes low and remains low until the terminal count is reached. The output then goes high until either the count register or the mode control register is reloaded.

b. Mode 1: Programmable one-shot. In this mode, the output of Counter 1 and/or Counter 2 will go low on the count following the rising edge of the GATE input from Port CC. The output will go high on terminal count. If a new count value is

PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter n
2	LSB	Count Register Byte Counter n
3	MSB	Count Register Byte Counter n

ALTERNATE PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter 0
2		Mode Control Word Counter 1
3		Mode Control Word Counter 2
4	LSB	Counter Register Byte Counter 1
5	MSB	Count Register Byte Counter 1
6	LSB	Count Register Byte Counter 2
7	MSB	Count Register Byte Counter 2
8	LSB	Count Register Byte Counter 0
9	MSB	Count Register Byte Counter 0

Figure 3-2. PIT Programming Sequence Examples

loaded while the output is low, it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse. The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

c. Mode 2: Rate generator. In this mode, the output of Counter 1 and/or Counter 2 will be low for one period of the clock input. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses, the present period will not be affected but the subsequent period will reflect the new value. The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter. When Mode 2 is set, the output will remain high until after the count register is loaded; thus, the count can be synchronized by software.

d. Mode 3: Square wave generator. Mode 3 is the primary operating mode for all three counters on the 8253. In this mode, the counter output remains high until one half of the count value in the count register has been decremented (for even numbers). The output then goes low for the other half of the count. If the value in the count register is odd, the counter output is high for (N+1)/2 counts, and low for (N-1)/2 counts.

e. Mode 4: Software triggered strobe. After this mode is set, the output will be high. When the count is loaded, the counter begins counting. On terminal count, the output will go low for one input clock period and then go high again. If the count register is reloaded between output pulses, the present count will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the count register will restart the counting for the new value.

f. Mode 5: Hardware triggered strobe. The counter will start counting on the rising edge of the gate input and the output will go low for one clock period when the terminal count is reached. The counter is retriggerable; the output will not go low until the full count after the rising edge of the gate input.

Table 3-4 provides a summary of the counter operation versus the gate inputs.

Table 3-4. PIT Counter Operation Vs. Gate Inputs

Signal Status / Modes	Low Or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output high immediately	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output high immediately	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

3-9. ADDRESSING

As listed in Table 3-5 the PIT uses the following four I/O addresses: D0, D2, D4, D6. Addresses D0, D2, and D4 respectively, are used in loading and reading the count in Counters 0, 1, and 2. Address D6 is used in writing the mode control word to the desired counter.

Table 3-5. PIT Register Addresses

CS	RD	WR	A_1	A_0	Activity	I/O Address (hex)
0	1	0	0	0	Load Counter No. 0	D0
0	1	0	0	1	Load Counter No. 1	D2
0	1	0	1	0	Load Counter No. 2	D4
0	1	0	1	1	Write Mode Word	D6
0	0	1	0	0	Read Counter No. 0	D0
0	0	1	0	1	Read Counter No. 1	D2
0	0	1	1	0	Read Counter No. 2	D4
0	0	1	1	1	No-Operation 3-State	D6
1	X	X	X	X	Disable 3-STate	—
0	1	1	X	X	No-Operation 3-State	—

NOTE: X = Irrelevant Bit

3-10. INITIALIZATION

To initialize the PIT chips, perform the following:

a. Write mode control word for Counter 0 to port D6. Note that all mode control words are written to D6, since the mode control word must specify which counter is being programmed. (Refer to Figure 3-1). Table 3-6 provides a sample subroutine for writing a mode control word for Counter 0.

b. Assuming the mode control word has selected a 2-byte load, load least-significant byte of count into Counter 0 at port D0. Table 3-6 provides a sample subroutine for loading a 2-byte count value.

c. Load most-significant byte of count into Counter 0 at port D0.

NOTE

Be sure to enter the downcount in two bytes if the counter was programmed for a two-byte entry in the mode control word. Similarly, enter the downcount value in BCD if the counter was so programmed.

d. Repeat steps a, b, and c for Counters 1 and 2.

Table 3-7 shows another example of a subroutine for writing a mode control word to Counter 0.

To read the count of a particular counter, proceed as follows (a typical counter read subroutine is given in Table 3-8):

a. Write counter register latch control word (Figure 3-3) to port D6. Control word specifies desired counter and selects counter latching operation. Bits D0 - D3 are irrelevant.

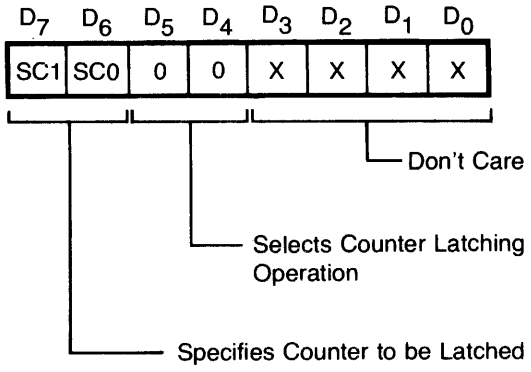


Figure 3-3. PIT Counter Register Latch Control Word Format

Table 3-6. Typical PIT Control Word Subroutine

```
;INTTMR INITIALIZES COUNTERS 0,1,2.
;COUNTERS 0 AND 1 ARE INITIALIZED AS INTERRUPT TIMERS.
;COUNTER 2 IS INITIALIZED AS BAUD RATE GENERATOR.
;ALL THREE COUNTERS ARE SET UP FOR 16-BIT OPERATION.
;DESTROYS-AL.

            PUBLIC    INTTMR

INTTMR:     MOV       AL,30H          ;MODE CONTROL WORD FOR COUNTER 0
            OUT       0D6H,AL
            MOV       AL,70H          ;MODE CONTROL WORD FOR COUNTER 1
            OUT       0D6H,AL
            MOV       AL,B6H          ;MODE CONTROL WORD FOR COUNTER 2
            OUT       0D6H,AL
            RET

            END
```

Table 3-7. Typical PIT Count Value Load Subroutine

```
;LOAD0 LOADS COUNTER 0 FROM CX, CH IS MSB, CL IS LSB.
;USES-D,E: DESTROYS—AL.

            PUBLIC    LOAD0

LOAD0:      MOV       AL,C            ;GET LSB
            OUT       0D0H,AL
            MOV       AL,CH           ;GET MSB
            OUT       0D0H,AL
            RET

            END
```

Table 3-8. Typical PIT Counter Read Subroutine

```
;READ1 READS COUNTER 1 ON-THE-FLY INTO CX. MSB IN CH, LSB IN CL.
;DESTROYS-AL,CX.

            PUBLIC    READ1

READ1:      MOV       AL,40H          ;MODE WORD FOR LATCHING COUNTER 1 VALUE
            OUT       0D6H,AL
            IN        AL,0D2H         :LSB OF COUNTER
            MOV       CL,A
            IN        AL,0D2H         ;MSB OF COUNTER
            MOV       CH,AL
            RET

            END
```

b. Perform a read operation of desired counter, refer to Table 3-5 for counter addresses.

NOTE

Be sure to read one or two bytes, whichever was specified in the initialization mode control word. For two bytes, read in the order specified.

3-11. CLOCK FREQUENCY/DIVIDE RATIO SELECTION. Table 2-5 lists the default and optional timer input frequencies to Counters 0 through 2. The timer input frequencies are divided by the counters to generate the OIT0 Interrupt Clock (Counter 0), OIT1 Clock (Counter 1), and the 8251A Baud Rate Clock (Counter 2).

Each counter must be programmed with a down-count number, or count value N. When count value N

is loaded into a counter, it becomes the clock divisor. To derive N for either synchronous or asynchronous RS 232C operation, use the procedures described in the following paragraphs.

Synchronous Mode. In the synchronous mode, the TXC and/or RXC rates equal the Baud rate. Therefore, the count value is determined by

$$N = C/B$$

where N is the count value,
B is the desired Baud rate, and
C is 1.23 MHz, the input clock frequency.

Thus, for a 4800 Baud rate, the required count value (N) is:

$$N = \frac{1.23 \times 10^6}{4800} = 256.$$

If the binary equivalent of count value N = 224 is loaded into Counter 2, then the output frequency is 4800 Hz, which is the desired clock rate for synchronous mode operation.

Asynchronous Mode. In the asynchronous mode, the TXC and/or RXC rates equal the Baud rate times one of the following multipliers: 16 or 64. Therefore, the count value is determined by:

$$N = C/BM$$

where N is the count value,
B is the desired Baud rate,
M is the Baud rate multiplier (16, or 64,) and
C is 1.23 MHz, the input clock frequency.

Thus, for a 4800 Baud rate, the required count value (N) is:

$$N = \frac{1.23 \times 10^6}{4800 \times 16} = 16$$

If the binary equivalent of count value N = 16 is loaded into Counter 2, then the output frequency is 4800 X 16 Hz, which is the desired clock rate for asynchronous mode operation. Count values (N) versus rate multiplier (M) for each Baud rate are listed in Table 3-9. A simplified version of this table, with hex notations is provided in Table 3-10.

NOTE

During initialization, be sure to load the count value (N) into the appropriate counter and the Baud rate multiplier (M) into the 8251A PCI.

Table 3-9. Count Values & Rate Multipliers

Baud Rate: (B)	*Count Value (N) For		
	M = 1	M = 16	M = 64
75	16384	1024	256
110	11171	698	175
150	8192	512	128
300	4096	256	64
600	2048	128	32
1200	1024	64	16
2400	512	32	8
4800	256	16	4
9600	128	8	
19200	64	4	
38400	32	2	
76800	16		

*Count Values (N) assume clock is 1.23 MHz. Double Count Values (N) for 2.46 MHz clock. Count Values (N) and Rate Multipliers (M) are in decimal.

Table 3-10. PIT Baud Rate Factors

Output Frequency In kHz	Baud Rate (Hz)			8253 PIT Baud Rate Factor (Hex Notation)	
	Synchronous	Asynchronous			
		÷16	÷64	MSB	LSB
153.6	—	9600	2400	00	07
76.8	—	4800	1200	00	0E
38.4	38400	2400	600	00	1C
19.2	19200	1200	300	00	38
9.6	9600	600	150	00	70
4.8	4800	300	75	00	E0
2.4	2400	150	—	01	C0
1.76	1760	110	—	02	63

Isosynchronous Mode. In some cases it is desirable to operate in a hybrid mode which involves transmitting data with the asynchronous format using a synchronous modem. This occurs when an increase in operating speed is required without a change in the basic protocol of the system. This hybrid technique is known as isosynchronous and involves the generation of the start and stop bits associated with the asynchronous format, while still using the modem clock for bit synchronization.

In the asynchronous mode the PCI can be programmed to accept clock rates of 16 or 64 times the required baud rate. Isosynchronous operation is a special case of asynchronous with the multiplier rate programmed as one instead of 16 or 64. Note that X1 operation is only valid if the clocks of the receiver and transmitter are synchronized.

3-12. RATE GENERATOR/INTERVAL TIMER. Table 3-11 shows the maximum and minimum rate

Table 3-11. PIT Rate Generator Frequencies and Timer Intervals

	Single Timer[1] (Counter 0)		Single Timer[2] (Counter 1)		Dual Timer[3] (0 and 1 in Series)	
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum
Rate Generator (frequency)	18.75 Hz	614.4 kHz	2.344 Hz	76.8 kHz	0.00029 Hz	307.2 kHz
Real-Time Interrupt (interval)	1.63 μsec	53.3 msec	13 μsec	426.67 msec	3.26 μsec	58.25 minutes

NOTES:
1. Assuming a 1.23-MHz clock input.
2. Assuming a 153.6-kHz clock input.
3. Assuming Counter 0 has 1.23-MHz clock input.

generator frequencies and timer intervals for Counters 0 and 1 when these counters respectively, have 1.23-MHz and 1.53.6-kHz clock inputs. The table also provides the maximum and minimum generator frequencies and time intervals that may be obtained by connecting Counters 0 and 1 in series.

3-13. INTERRUPT TIMER. To program an interval timer for an interruption terminal count, program the appropriate timer for the correct operating mode (Mode 0) in the control word. Then load the count value (N), which is derived by:

$$N = TC$$

where N is the count value for Counter 1,
T is the desired interrupt time interval in seconds, and
C is the internal clock frequency (Hz).

Table 3-12 shows the count value (N) required for several time intervals (T) that can be generated for Counters 0 and 1.

Table 3-12. PIT Timer Intervals & Timer Counts

T	N*
10 μsec	12
100 μsec	123
1 msec	1229
10 msec	12288
50 msec	61440

*Count Values (N) assume clock is 1.23 MHz. Count Values (N) are in decimal.

3-14. 8251A PCI PROGRAMMING

The PCI converts parallel output data into virtually any series output data format (including IBM Bi-Sync) for half- or full-duplex operation. The PCI also converts serial input data into parallel data format.

Prior to transmitting or receiving data, the PCI must be loaded with a set of control words. These control words, which define the complete functional operation of the PCI, must immediately follow a reset (internal or external). The control words are either a Mode instruction or a Command instruction.

3-15. MODE INSTRUCTION FORMAT

The Mode instruction word defines the general characteristics of the PCI and must follow a reset operation. Once the Mode instruction word has been written into the PCI, sync characters or command instructions may be inserted. The Mode instruction word defines the following:

a. For Sync Mode:
   (1) Character length
   (2) Parity enable
   (3) Even/odd parity generation and check
   (4) External sync detect
   (5) Single or double character sync

b. For Async Mode:
   (1) Baud rate factor (X16 or X64)
   (2) Character length
   (3) Parity enable

Instruction word and data transmission formats for synchronous and asynchronous modes are shown in Figures 3-4 through 3-8.

3-16. SYNC CHARACTERS

Sync characters are written to the PCI in the synchronous mode only. The PCI can be programmed for either one or two sync characters; the format of the sync characters is at the option of the programmer.

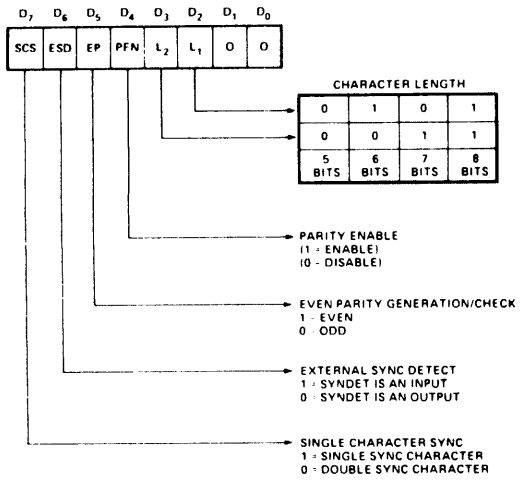


Figure 3-4. PCI Synchronous Mode Instruction Word Format

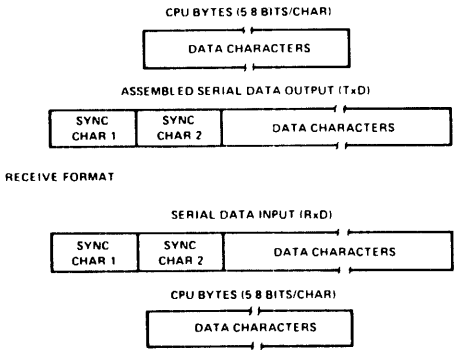


Figure 3-5. PCI Synchronous Mode Transmission Format

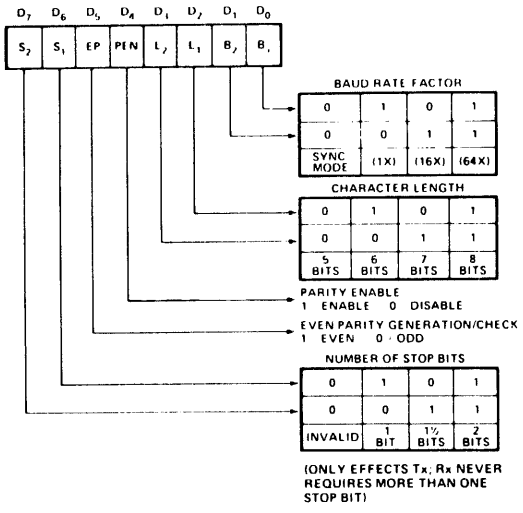


Figure 3-6. PCI Asynchronous Mode Instruction Word Format

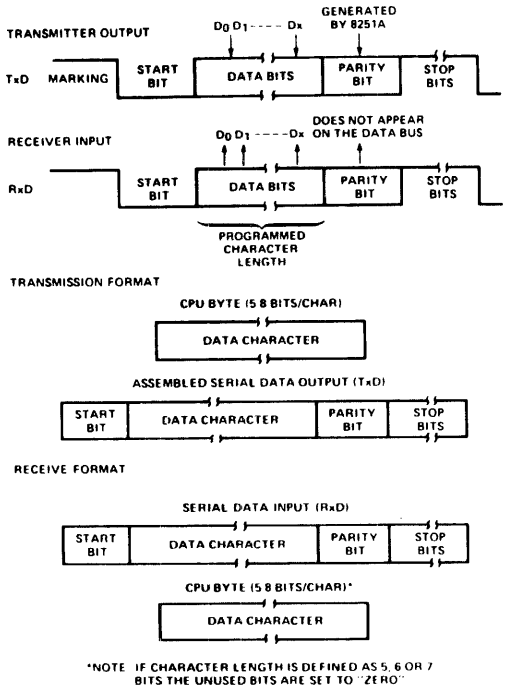


Figure 3-7. PCI Asynchronous Mode Transmission Format

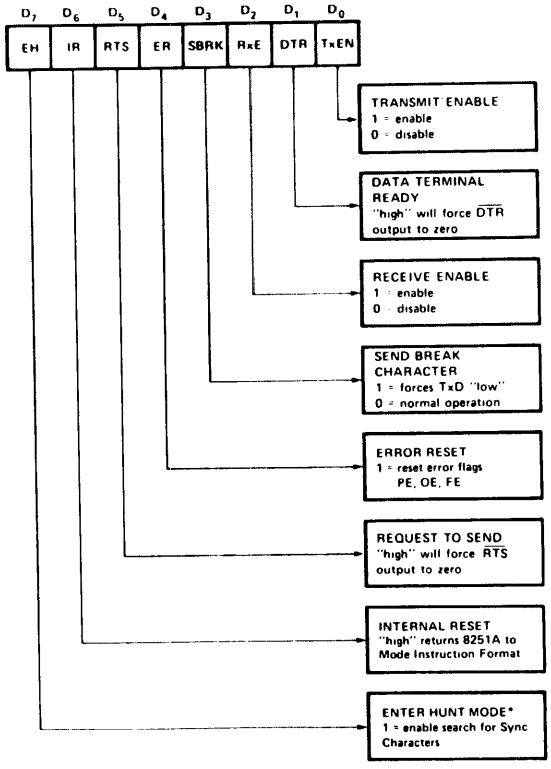


Figure 3-8. PCI Command Instruction Word Format

3-17. COMMAND INSTRUCTION FORMAT

The Command instruction word shown in Figure 3-8 controls the operation of the addressed PCI. A Command instruction must follow the mode and/or sync words and, once the Command instruction is written, data can be transmitted or received by the PCI.

It is not necessary for a Command instruction to precede all data transactions; only those transactions that require a change in the Command instruction. An example is a change in the enable transmit bit or enable receive bit. Command instructions can be written to the PCI at any time after one or more data operations.

After initialization, always read the PCI status and check for the TxRDY bit prior to writing either data or command words to the PCI. This ensures that any prior input is not overwritten and lost. Note that issuing a Command instruction with bit 6 (IR) set will return the PCI to the Mode instruction format.

3-18. RESET

To change the Mode instruction word, the PCI must receive a Reset command. This can be either a hardware reset or a reset generated by bit 6 of the Command Instruction. The next word written to the PCI after a Reset command is assumed to be a Mode instruction. Similarly, for sync mode, the next word after a Mode instruction is assumed to be one or more sync characters. All control words written into the PCI after the Mode instruction (and/or the sync character) are assumed to be Command instructions.

3-19. ADDRESSING

The PCI device uses two consecutive pairs of addresses. The lower of the two addresses in each pair is used to read and write I/O data; the upper address in each pair is used to write mode and command words and to read the PCI status. (Refer to Table 3-13).

Table 3-13. PCI Address Assignments

I/O Address (hexadecimal)	Command	Function	Direction
DA or DE	OUTPUT	CONTROL	CPU → PCI
D8 or DC	OUTPUT	DATA	CPU → PCI
DA or DE	INPUT	STATUS	PCI → CPU
D8 or DC	INPUT	DATA	PCI → CPU

3-20. INITIALIZATION

A typical PCI initialization and I/O data sequence is presented in Figure 3-7. The PCI device is initialized in four steps:

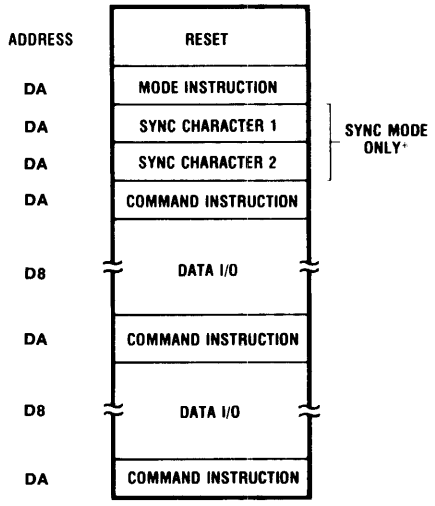
a. Reset PCI to Mode instruction format.

b. Write four sets of zeros to the PCI. This will prevent spurious operation.

c. Write Mode instruction word. One function of mode word is to specify synchronous or asynchronous operation.

d. If synchronous mode is selected write one or two sync characters as required.

e. Write Command instruction word.



*The second sync character is skipped if Mode instruction has programmed PCI to single character internal sync mode. Both sync characters are skipped if Mode instruction has programmed PCI to async mode.

Figure 3-9. Typical PCI Initialization & Data I/O Sequence

To avoid spurious interrupts during PCI initialization, disable the PCI interrupt. This can be done by either masking the appropriate interrupt request input at the 8259A PIC or by disabling the 8086 microprocessor interrupts by executing a CLI instruction.

First, reset the PCI device by writing a Command instruction to Port 00DA (or 00DE). The Command instruction must have bit 6 set (IR = 1); all other bits are immaterial.

NOTE

This reset procedure should be used only if the PCI has been completely initialized, or the initialization procedure has reached the point wthat the PCI is ready to receive a Command word. For example, if the reset command is written when the initialization sequence calls for a sync character, then subsequent programming will be in error.

Next write a Mode instruction word to the PCI. (See Figure 3-4 through 3-7.) A typical subroutine for writing both Mode and Command instructions is given in Table 3-14.

If the PCI is programmed for the synchronous mode, write one or two sync characters depending on the transmission format.

Finally, write a Command instruction word to the PCI. Refer to Figure 3-8 and Table 3-14.

IMPORTANT: During initialization, the 8251A PCI requires a minimum recovery time of 6.5 microseconds (16 PCI clock cycles) between back-to-back writes in order to set up its internal registers. This recovery time can be satisfied by the CPU performing several dummy instructions between the back-to-back writes to the 8251A to create a minimum delay of 6.5 microseconds. The following example will create a delay of approximately 7.2 microseconds.

```
        MOV     AL,04EH     ;PCI MODE WORD
        OUT     0DAH,AL     ;FIRST PCI WRITE
        MOV     CX,3        ;DELAY
TAG:    LOOP    TAG         ;DELAY
        MOV     AL,037H     ;PCI COMMAND WORD
        OUT     0DAH,AL     ;SECOND PCI WRITE
```

This precaution applies only to the PCI initialization and does not apply otherwise.

3-21. OPERATION

Normal operating procedures use data I/O read and write, status read, and Command instruction write operations. Programming and addressing procedures for the above are summarized in following paragraphs.

NOTE

After the PCI has been initialized, always check the status of the TXRDY bit *prior* to writing data or writing a new command word to the PCI. The TXRDY bit *must* be *true* to prevent overwriting and subsequent loss of command or data words. The TXRDY bit is inactive until initialization has been completed; do not check TXRDY until after the command word, which concludes the initialization procedure, has been written.

Prior to any operating change, a new command word must be written with command bits changed as appropriate. (Refer to Figure 3-8 and Table 3-14.)

Data Input/Output. For data receive or transmit operations, perform a read or write, respectively, to the PCI. Tables 3-15 and 3-16 provide examples of typical character read and write subroutines.

During a normal transmit operation, the PCI generates a Transmit Ready (TXRDY) signal that indicates that the PCI is ready to accept a data character for transmission. TXRDY is automatically reset when the CPU loads a character into the PCI.

Similarly, during a normal receive operation, the PCI generates a Receive Ready (RXRDY) signal that indicates that a character has been received and is ready for input to the CPU. RXRDY is automatically reset when a character is read by the CPU.

Table 3-14. Typical PCI Mode or Command Instruction Subroutine

```
;CMD 2 OUTPUTS CONTROL WORD TO USART FROM AL REGISTER.
;USES-AL, STAT0; DESTROYS-NOTHING.

        PUBLIC  CMD2,51INT
        EXTRN   STAT0

CMD2:   PUSH    AX
        PUSH    F
LP:     CALL    STAT0
        AND     AL,1            ;CHECK TXRDY
        JZ      LP              ;TXRDY MUST BE TRUE
        POPF
        POP     AX
51INT:  OUT     0DAH,AL         ;ENTER HERE FOR INITIALIZATION
        RET

        END
```

Table 3-15. Typical PCI Data Character Read Subroutine

```
;RX1 READS DATA CHARACTER FROM USART INTO REG AL.
;USES-STAT0; DESTROYS-AL, FLAGS.

        PUBLIC  RX1,RXA1
        EXTRN   STAT0

RX1:    CALL    STAT0
        AND     AL,2            ;CHECK FOR RXRDY TRUE
        JZ      RX1
RXA1:   IN      AL,0D8H         ;ENTER HERE IF RXRDY IS TRUE
        RET

        END
```

Table 3-16. Typical PCI Data Character Write Subroutine

```
;TX1 WRITES DATA CHARACTER FROM REG AL TO USART.
;USES-AL, STAT0; DESTROYS-FLAGS.

        PUBLIC  TX1,TXA1
        EXTRN   STAT0

TX1:    PUSH    AX
TX11:   CALL    STAT0
        AND     AL,1            ;CHECK FOR TXRDY TRUE
        JZ      TX11
        POP     AX
TXA1:   OUT     0D8H,AL         ;ENTER HERE IF TXRDY IS TRUE
        RET

        END
```

The TXRDY and RXRDY outputs of the PCI are available at the priority interrupt jumper matrix. If, for instance, TXRDY and RXRDY are input to the 8259A PIC, the PIC resolves the priority and interrupts the CPU. TXRDY and RXRDY are also available in the status word. (Refer to paragraph 3-23.)

Status Read. The CPU can determine the status of a serial I/O port by issuing an I/O Read Command to the upper port (00DA or 00DE) of the PCI. The format of the status word is shown in Figure 3-10. A typical status read subroutine is given in Table 3-17.

3-22. 8255A PPI PROGRAMMING

The iSBC 86/05 board has a total of 24 parallel I/O lines, grouped into three ports: C8, CA, and CC. All lines exit the board via connector J1. One 8255A PPI device is used to control all three ports. Line identification is provided in Table 2-23.

Each of the three parallel I/O ports may be programmed independently. However, as implemented on the iSBC 86/05 board, some lines have restricted use in certain modes. The modes allowed on the iSBC 86/05 board are listed in Table 3-18. Notice that each half of port CC may be programmed independently. These configurations are shown in Table 3-21, along with configurations for ports C8 and CA.

Default jumpers set the port C8 bus transceivers to the output (transmit) mode. Optional jumper connections allow the bus transceivers to be set to either the input mode or a bit-programmable input/output mode. Refer to Table 2-9 for complete jumper information.

Ports CA and CC do not have bus transceivers installed at the factory. Line drivers or terminators can be installed for these ports as described in Section 2-10.

In order to use any of the parallel port lines, the 8255A PPI device must first be initialized and programmed for the desired mode and direction of data flow. Sections 3-23 through 3-26 provide this information.

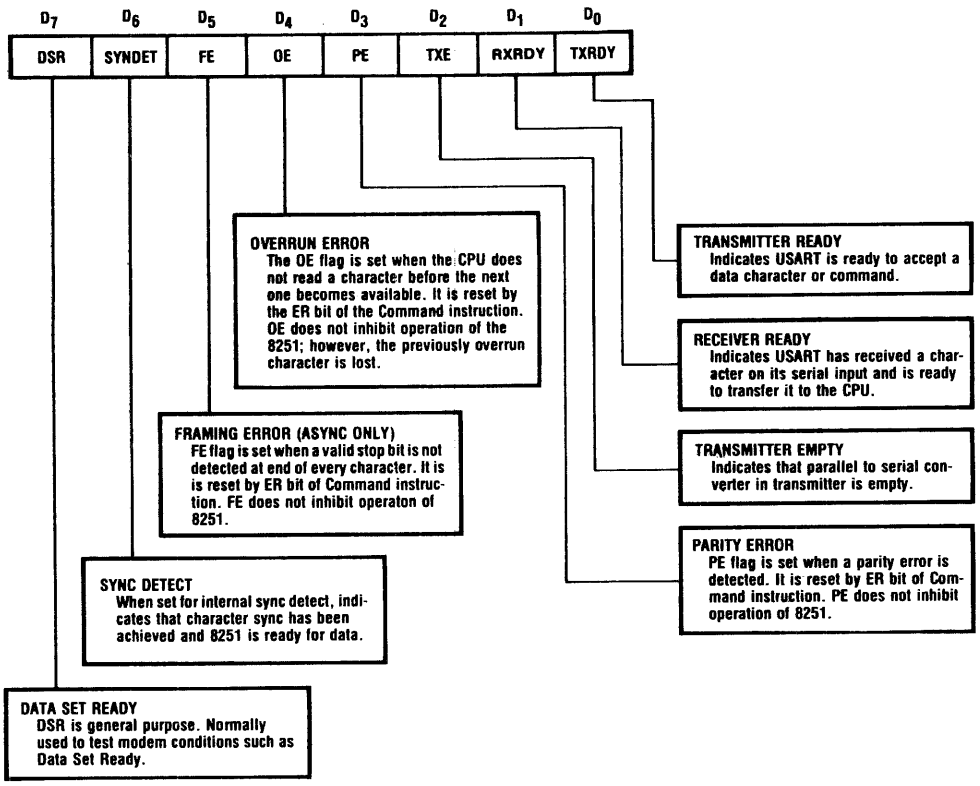


Figure 3-10. PCI Status Read Format

Table 3-17. Typical PCI Status Read Subroutine

```
;STAT0 READS STATUS FROM USART.
;DESTROYS-AL.

            PUBLIC    STAT0

STAT0:      IN        AL,0DEH          ;GET STATUS
            RET

            END
```

3-23. CONTROL WORD FORMAT

The control word format shown in Figure 3-11 is used to initialize each PPI port. Group A (control word bits 3 through 6) defines the operating mode for port A and the upper four bits of port C. Group B (control word bits 0 through 2) defines the operating mode for port B and the lower four bits of port C. (Refer to Table 3-19 for port identification). Bit 7 of the control word controls the mode set flag. Control words are sent to port CE (Table 3-19). There are restrictions associated with the use of certain ports in modes 1 and 2. Refer to Table 2-6 for restrictions.

Table 3-18. Parallel Port Configurations

Port C8 Mode 0, input Mode 0, output (latched) Mode 1, input (strobed) Mode 1, output (latched) Mode 2, bidirectional
Port CA Mode 0, input Mode 0, output (latched) Mode 1, input (strobed) Mode 1, ouput (latched)
Port CC * Mode 0, 8-bit input Mode 0, 8-bit output (latched) Mode 0, split (4-bit input, 4-bit output)
*Control mode may depend on mode of other ports; see table 2-10.

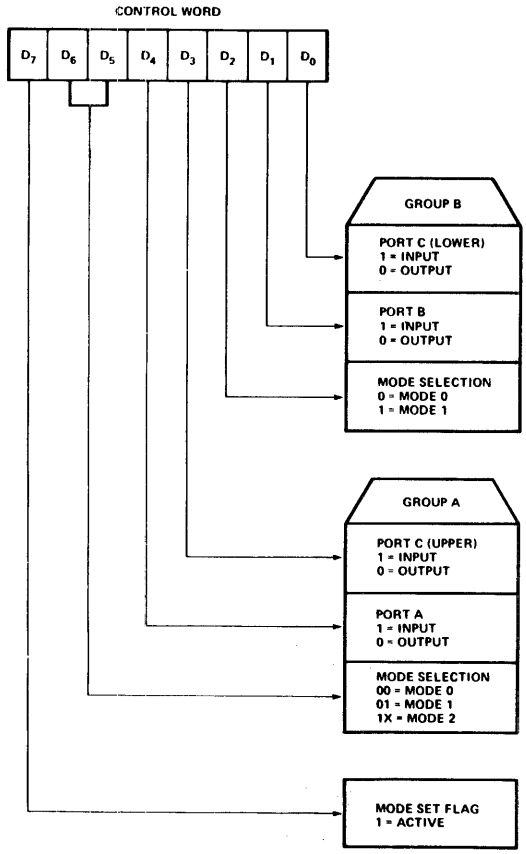


Figure 3-11. PPI Control Word Format

Table 3-19. Parallel Port I/O Addresses

8255A Device Port	Eight-Bit Address (hexadecimal)
8255A Port (A)	C8
8255A Port (B)	CA
8255A Port (C)	CC
8255A Control	CE For I/O write only

3-24. ADDRESSING

The PPI uses four consecutive *even* addresses (00C8 through 00CE) for data transfer, obtaining the status of Port C (00CC), and for port control. (Refer to Table 3-19.)

3-25. INITIALIZATION

To initialize the PPI, write a control word to port 00CE. Refer to Figure 3-11 and Table 3-20 and assume that the control word is 92 (hexadecimal). This initializes the PPI as follows:

a. Mode Set Flag active
b. Port A (00C8) set to Mode 0 Input
c. Port C (00CC) upper set to Mode 0 Output
d. Port B (00CA) set to Mode 0 Input
e. Port C (00CC) lower set to Mode 0 Output

3-26. OPERATION

The primary considerations in determining how to operate each of the three I/O ports are:

a. Choice of operating mode (as defined in Table 3-18);
b. Direction of data flow (input, output or bidirectional), (see Table 3-23); and
c. Choice of driver/terminator networks.

After the PPI has been initialized, the operation is completed by simply performing a read or a write to the appropriate port.

A typical read subroutine for Port A is given in Table 3-21.

A typical write subroutine for Port C is given in Table 3-22. As shown in Figure 3-13, any of the Port C bits can be selectively set or cleared by writing a control word to Port 00CE.

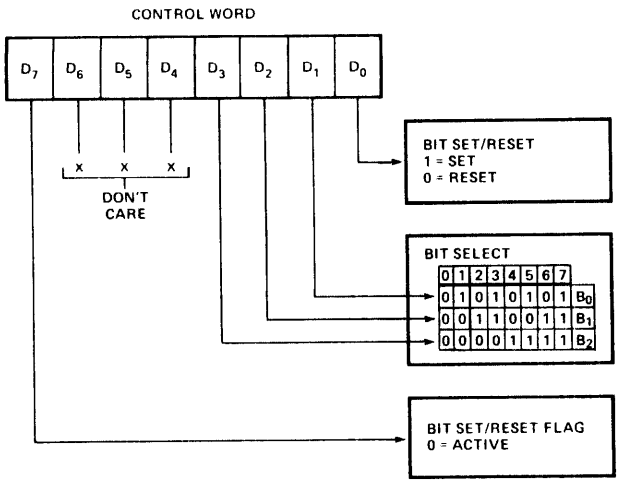


Figure 3-12. PPI Port C Bit Set/Reset Control Word Format

Single Bit Set/Reset Feature

Any of the eight bits of Port C (board port CC) can be Set or Reset using a single output instruction (see Figure 3-12). This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Mode Combinations

Table 3-23 summarizes the various mode combinations possible with ports A and B of each PPI, and indicates how each port C bit can be used. This table can serve as a useful starting point for selecting your particular configuration. Once you select the desired mode combination and the port C bit assignments are made, refer to the jumper configuration table (2-6) for implementation details.

Table 3-20. Typical PPI Initialization Subroutine

```
;INTPAR INITIALIZES PARALLEL PORT MODES.
;DESTROYS-AL.

        PUBLIC  INTPAR

INTPAR: MOV     AL,92H          ;MODE WORD TO PPI PORT A&B IN,C OUT
        OUT     0CEH, AL
        RET

        END
```

Table 3-21. Typical PPI Port Read Subroutine

```
;AREAD READS A BYTE FROM PORT A INTO REG AL.
;DESTROYS-AL.

        AREAD

AREAD:  IN      AL,0C8H         ;GET BYTE
        RET

        END
```

Table 3-22. Typical PPI Port Write Subroutine

```
;COUT OUTPUTS A BYTE FROM REG AL TO PORT C.
;USES-AL; DESTROYS-NOTHING.

        PUBLIC  COUT

COUT:   OUT     0CCH,AL         ;OUTPUT BYTE
        RET

        END
```

Table 3-23. Parallel I/O Interface Configurations

Configuration Number	PPI Port A (C8)	PPI Port B (CA)	PPI Port C (CC) Lower				PPI Port C (CC) Upper			
			C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
1	MODE 0-IN	MODE 0-I/O		— I/O —				— I/O —		
2	MODE 0-OUT	MODE 0-I/O		— I/O —				— I/O —		
3	MODE 0-IN	MODE 1-I/O	R	R	R	I	O	O	O	U
4	MODE 0-IN	MODE 1-I/O	R	R	R	O	I	I	I	U
5	MODE 0-OUT	MODE 1-I/O	R	R	R	I	O	O	O	U
6	MODE 0-OUT	MODE 1-I/O	R	R	R	O	I	I	I	U
7	MODE 1-IN	MODE 0-I/O	I	I	I	R	R	R	O	O
8	MODE 1-IN	MODE 0-I/O	O	O	O	R	R	R	I	I
9	MODE 1-OUT	MODE 0-I/O	I	I	I	R	O	O	R	R
10	MODE 1-OUT	MODE 0-I/O	O	O	O	R	I	I	R	R
11	MODE 1-IN	MODE 1-I/O	R	R	R	R	R	R	I	I
12	MODE 1-IN	MODE 1-I/O	R	R	R	R	R	R	O	O
13	MODE 1-OUT	MODE 1-I/O	R	R	R	R	I	I	R	R
14	MODE 1-OUT	MODE 1-I/O	R	R	R	R	O	O	R	R
15	MODE 2-B	MODE 0-I/O	U	I	I	R	R	R	R	R
16	MODE 2-B	MODE 0-I/O	U	O	O	R	R	R	R	R
17	MODE 2-B	MODE 1-I/O	R	R	R	R	R	R	R	R

NOTES:
I - INPUT
O - OUTPUT
I/O - INPUT OR OUTPUT
B - BIDIRECTIONAL
R - RESERVED
U - No unused drivers/terminators available. These bits may be used, however, to connect to the serial I/O interface or the Interval Timer.

3-27. 8259A PIC PROGRAMMING

The 8259A PIC functions as an overall manager in an interrupt-driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and may issue an interrupt to the CPU based on this determination.

The on-board master 8259A PIC handles up to eight vectored priority interrupts and has the capability of expanding the number of priority interrupts by cascading one or more of its interrupt input lines with slave 8259A PIC's. (Refer to paragraph 2-14.)

The basic functions of the PIC are to (1) resolve the priority of interrupt requests, (2) issue a single interrupt request to the CPU based on that priority, and (3) send the CPU a vectored restart address for servicing the interrupting device.

3-28. INTERRUPT PRIORITY MODES

The PIC can be programmed to operate in one of the following modes:

a. Nested Mode
b. Fully Nested Mode
c. Automatic Rotating Mode
d. Specific Rotating Mode
e. Special Mask Mode
f. Poll Mode

3-29. NESTED MODE. In this mode, the PIC input signals are assigned a priority from 0 through 7. The PIC operates in this mode unless specifically programmed otherwise. Interrupt IR0 has the highest priority and IR7 has the lowest priority. When an interrupt is acknowledged, the highest priority request is available to the CPU. Lower priority interrupts are inhibited; higher priority interrupts will be able to generate an interrupt that will be acknowledged if the CPU has enabled its own

interrupt input through software. The End-Of-Interrupt (EOI) command from the CPU is required to reset the PIC for the next interrupt.

3-30. FULLY NESTED MODE. This mode is used only when one or more PIC's are slaved to the master PIC, in which case the priority is conserved within the slave PIC's.

The operation in the fully nested mode is the same as the nested mode except as follows:

a. When an interrupt from a slave PIC is being serviced, that particular PIC is not locked out from the master PIC priority logic. That is, further interrupts of higher priority within this slave PIC will be recognized and the master PIC will initiate an interrupt to the CPU.

b. When exiting the interrupt service routine, the software must check to determine if another interrupt is pending from the same slave PIC. This is done by sending an End-Of-Interrupt (EOI) command to the slave PIC and then reading its In-Service (IS) register. If the IS register is clear (empty), an EOI command is sent to the master PIC. If the IS register is not clear (interrupt pending), no EOI command should be sent to the master PIC.

3-31. AUTOMATIC ROTATING MODE. In this mode, the interrupt priority rotates. Once an interrupt on a given input is serviced, that interrupt assumes the lowest priority. Thus, if there are a number of simultaneous interrupts, the priority will rotate among the interrupts in numerical order. For example, if interrupts IR4 and IR6 request service simultaneously, IR4 will receive the highest priority. After service, the priority level rotates so that IR4 has the lowest priority and IR5 assumes the highest priority. In the worst case, seven other interrupts are serviced before IR4 again has the highest priority. Of course, if IR4 is the only request, it is serviced promptly. The priority shifts when the PIC receives an End-Of-Interrupt (EOI) command.

3-32. SPECIFIC ROTATING MODE. In this mode, the software can change interrupt priority by specifying the bottom priority, which automatically sets the highest priority. For example, if IR5 is assigned the bottom priority, IR6 assumes the highest priority. In specific rotating mode, the priority can be rotated by writing a Specific Rotate at EOI (SEOI) command to the PIC. This command contains the BCD code of the interrupt being serviced; that interrupt is reset as the bottom priority. In addition, the bottom priority interrupt can be fixed at any time by writing a command word to the appropriate PIC.

3-33. SPECIAL MASK MODE. One or more of the eight interrupt request inputs can be individually masked during the PIC initialization or at any subsequent time. If an interrupt is masked while it is being serviced, lower priority interrupts are inhibited. There are two ways to enable the lower priority interrupts:

a. Write an End-Of-Interrupt (EOI) command.

b. Set the Special Mask Mode.

The Special Mask Mode is useful when one or more interrupts are masked. If for any reason an input is masked while it is being serviced, the lower priority interrupts are disabled. However, it is possible to enable the lower priority interrupt with the Special Mask Mode. In this mode, the lower priority lines are enabled until the Special Mask Mode is reset. Higher priorities are not affected.

3-34. POLL MODE. In this mode the CPU internal Interrupt Enable flip-flop is clear (interrupts disabled) and a software subroutine is used to initiate a Poll command. In the Poll Mode, the addressed PIC treats an I/O Read Command as an interrupt acknowledge, sets its In-Service flip-flop if there is a pending interrupt request, and reads the priority level. This mode is useful if there is a common service routine for several devices.

3-35. STATUS READ

Interrupt request inputs are handled by the following three internal PIC registers:

a. Interrupt Request Register (IRR), which stores all interrupt levels that are requesting service.

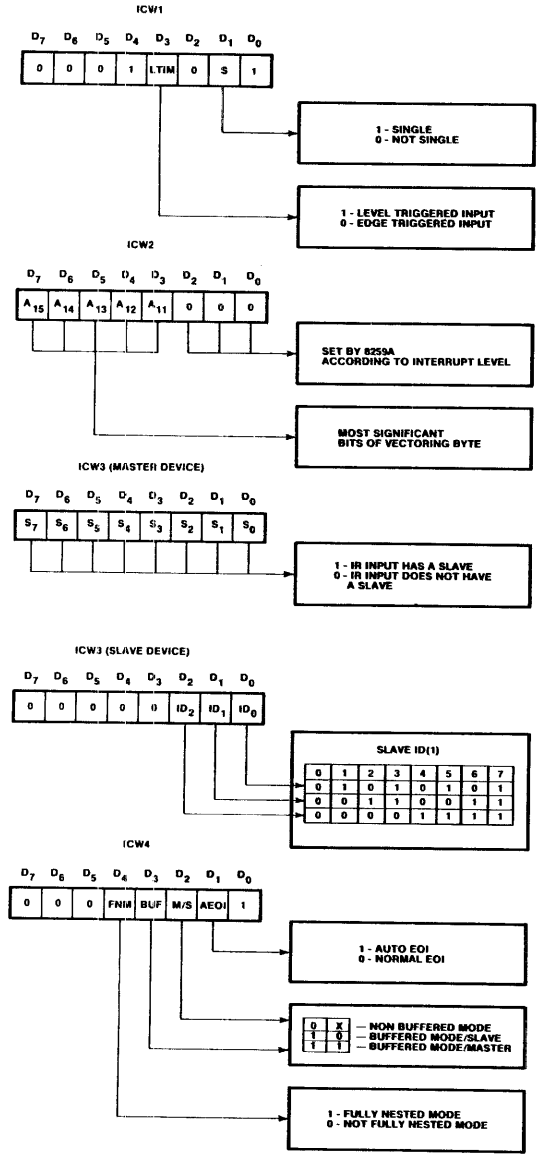
b. In-Service Register (ISR), which stores all interrupt levels that are being serviced.

c. Interrupt Mask Register (IMR), which stores the interrupt request lines which are masked.

These registers can be read by writing a suitable command word and then performing a read operation.

3-36. INITIALIZATION COMMAND WORDS

The on-board master PIC and each slave PIC requires a separate initialization sequence to work in a particular mode. The initialization sequence requires three Initialization Command Words (ICW's) for a single PIC system and requires four ICW's for a master PIC with one to eight slaves. The ICW formats are shown in Figure 3-13.



NOTE 1: SLAVED ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.
NOTE 2: X INDICATED "DON'T CARE".

Figure 3-13. PIC Initialization Command Word Formats

The first Initialization Command Word (ICW1), which is required in all modes of operation, consists of the following:

a. Bits 0 and 4 are both 1's and identify the word as ICW1 for an 8086 CPU operation.

b. Bit 1 denotes whether or not the PIC is employed in a multiple PIC configuration. For a single master PIC configuration (no slaves), bit 1=1; for a master with one or more slaves, bit 1=0.

NOTE

Bit 1=0 when programming a slave PIC.

c. Bit 3 establishes whether the interrupts are requested by a positive-true level input or requested by a low-to-high input. This applies to all input requests handled by the PIC. In other words, if bit 3=1, a low-to-high transition is required to request an interrupt on any of the eight levels handled by the PIC.

The second Initialization Command Word (ICW2) represents the vectoring byte (identifier) and is required by the 8086 CPU during interrupt processing. ICW2 consists of the following:

a. Bits D3-D7 (A11-A15) represent the five most significant bits of the vector byte. These are supplied by the programmer.

b. Bits D0-D2 represent the interrupt level requesting service. These bits are provided by the 8259A during interrupt processing. These bits should be programmed as 0's when initializing the PIC.

NOTE

The 8086 CPU multiplies the vector byte by four. This value is then used by the CPU as the vector address.

Table 3-24 lists the vector byte contents for interrupts IR0-IR7.

Table 3-24. Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	A15	A14	A13	A12	A11	1	1	1
IR6	A15	A14	A13	A12	A11	1	1	0
IR5	A15	A14	A13	A12	A11	1	0	1
IR4	A15	A14	A13	A12	A11	1	0	0
IR3	A15	A14	A13	A11	A10	0	1	1
IR2	A15	A14	A13	A12	A11	0	1	0
IR1	A15	A14	A13	A12	A11	0	0	1
IR0	A15	A14	A13	A12	A11	0	0	0

The third Initialization Command Word (ICW3) is required only if bit 1=0 in ICW1, specifying that multiple PIC's are used; i.e., one or more PIC's are slaved to the on-board master PIC. ICW3 programming can be in one of two formats: master mode format and slave mode format.

a. For master mode, the D0-D7 (S0-S7) bits correspond to the IR0-IR7 bits of the master PIC. For example,if a slave PIC is connected to the master PIC IR3 input, code bit 3=1.

b. For a slave PIC, the D0-D2 (ID0-ID2) bits identify the master IR line that the slave PIC is connected to. The slave compares its cascade input (generated by the master PIC) with these bits and, if they are equal, the slave releases an interrupt vector byte upon the reception of the second INTA during interrupt processing. For example, if a slave is connected to the master interrupt line IR5, code bits ID0-ID2=101.

The fourth Initialization Command Word (ICW4), which is required for all modes of operation, consists of the following:

a. Bit D0 is a 1 to identify that the word is for an 8086 CPU.

b. Bit D1 (AEO1) programs the end-of-interrupt function. Code bit 1=1 if an EOI is to be automatically executed (hardware). Code bit 1=0 if an EOI command is to be generated by software before returning from the service routine.

c. Bit D2 (M/S) specifies if ICW4 is addressed to a master PIC or a slave PIC. For example, code bit 2=1 in ICW4 for the master PIC. If bit D3 (BUF) is zero, bit D2 has no function.

d. Bit D3 (BUF) specifies whether the 8259A is operating in the buffered or nonbuffered mode. For example, code bit 3=1 for buffered mode.

   The master PIC in an iSBC 86/12A, with or without slaves, must be operated in the buffered mode.

e. Bit D4 (FNM) programs the nested or fully nested mode. (Refer to paragraph 3-29 and 3-30).

In summary, three or four ICW's are required to initialize the master and each slave PIC. Specifically

- Master PIC — No Slaves
  - ICW1
  - ICW2
  - ICW4
- Master PIC — With Slave(s)
  - ICW1
  - ICW2
  - ICW3
  - ICW4
- Each Slave PIC
  - ICW1
  - ICW2
  - ICW3
  - ICW4

3-37. OPERATION COMMAND WORDS

After being initialized, the master and slave PIC's can be programmed at any time for various operating modes. The Operation Command Word (OCW) formats are shown in Figure 3-14 and discussed in paragraphs 3-40.

3-38. ADDRESSING

The master PIC uses Port 00C0 or 00C2 to write initialization and operation command words and Port 00C4 or 00C6 to read status, poll, and mask bytes. Addresses for the specific functions are provided in Table 3-3.

Slave PIC's, if employed, are accessed via the Multibus interface and their addresses are determined by the hardware designer.

3-39. INITIALIZATION

To initialize the PIC's (master and slaves), proceed as follows (Table 3-25 provides a typical PIC initialization subroutine for a PIC operated in the non-bus vectored mode; Table 3-26 and 3-27 are typical master PIC and slave PIC initialization subroutines for the bus vectored mode):

a. Disable system interrupts by executing a CLI (Clear Interrupt Flag) instruction.

b. Initialize master PIC by writing ICW's in the following sequence:
   (1) Write ICW1 to Port 00C0 and ICW2 to Port 00C2.
   (2) If slave PIC's are used, write ICW3 and ICW4 to Port 00C2. If no slave PIC's are used, omit ICW3 and write ICW4 only to Port 00C2.

c. Initialize *each* slave PIC by writing ICW's in the following sequence: ICW1, ICW2, ICW3, and ICW4.

d. Enable system interrupts by executing an STI (Set Interrupt Flag) instruction.

NOTE

Each PIC independently operates in the nested mode (paragraph 3-29) after initialization and before an Operation Control Word (OCW) programs it otherwise.

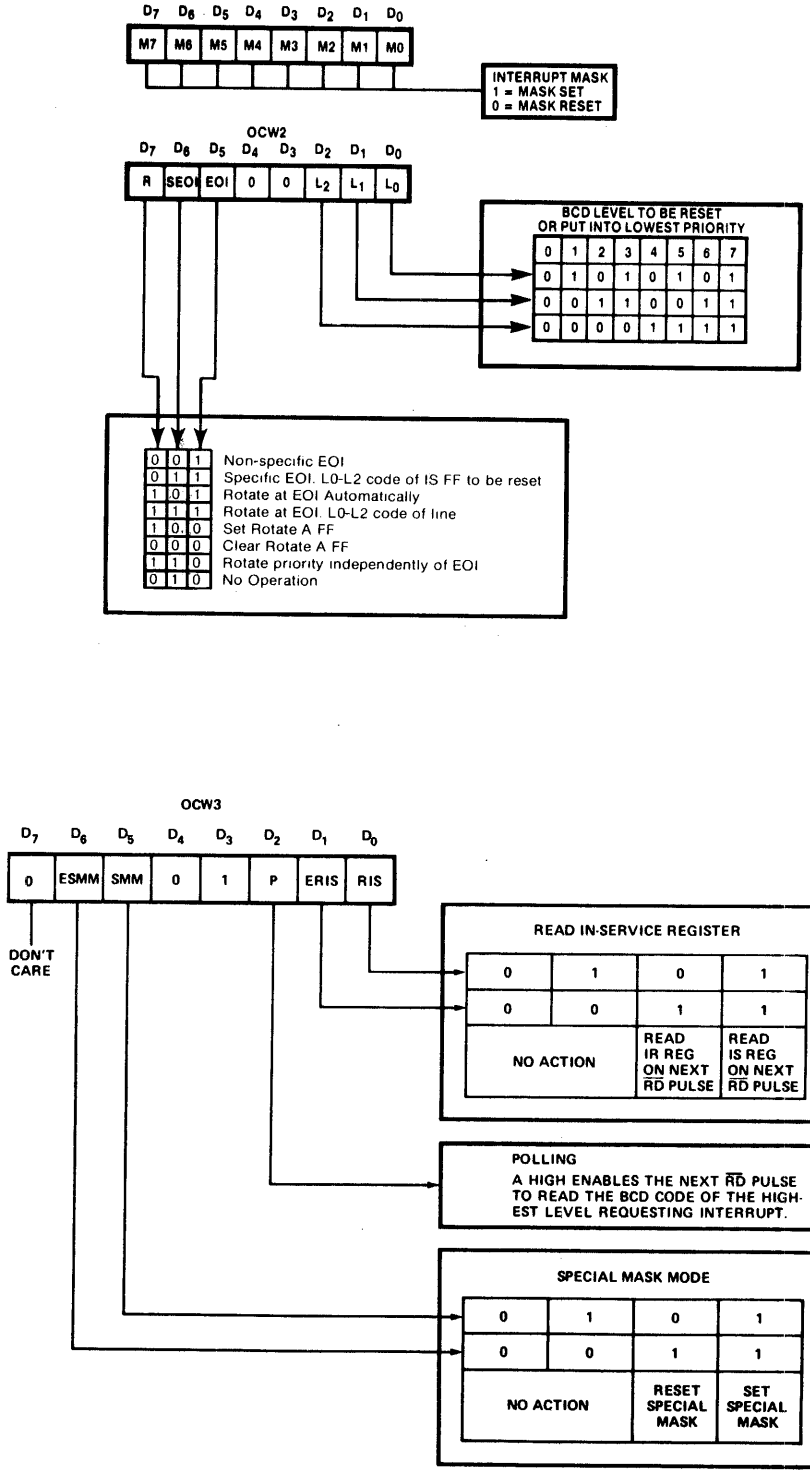


Figure 3-14. PIC Operation Control Word Formats

Table 3-25. Typical PIC Initialization Subroutine (NBV Mode)

```
;INT59 INITIALIZES THE PIC. A 32-BYTE ADDRESS BLOCK BEGINNING WITH
;00020H IS SET UP FOR INTERRUPT SERVICE ROUTINES.
;PIC MASK IS SET, DISABLING ALL PIC INTERRUPTS.
;PIC IS IN FULLY NESTED MODE, NON-AUTO EOI.
;USES SMASK; DESTROYS-A.

          PUBLIC    INT59
          EXTRN     SMASK

INT59:    MOV       AL,13H
          OUT       0C0H,AL          ;ICW1 TO PIC
          MOV       AL,08H
          OUT       0C2H,AL          ;ICW2 TO PIC
          MOV       AL,1DH
          OUT       0C2H,AL          ;ICW4 TO PIC
          MOV       AL,0FFH
          CALL      SMASK
          RET

          END
```

Table 3-26. Typical Master PIC Initialization Subroutine (BV Mode)

```
;INTMA INITIALIZES MASTER PIC WITH A SINGLE SLAVE ATTACHED
;TO THE 0 LEVEL INTERRUPT INPUT.
;PIC MASK IS SET WITH ALL PIC INTERRUPTS DISABLED.
;MASTER PIC IS FULLY NESTED, NON-AUTO EOI.
;USES SMASK; DESTROYS AL.

          PUBLIC    INTMA
          EXTRN     SMASK

INTMA:    MOV       AL,11H           ;ICW1
          OUT       0C0H,AL
          MOV       AL,08H           ;ICW2
          OUT       0C2H,AL
          MOV       AL,01H           ;ICW3
          OUT       0C2H,AL
          MOV       AL,1DH           ;ICW4
          OUT       0C2H,AL
          MOV       AL,0FFH
          CALL      SMASK
          RET

          END
```

Table 3-27. Typical Slave PIC Initialization Subroutine (BV Mode)

```
;INTSL INITIALIZES A SLAVE PIC LOCATED AT ADDRESS BLOCK
;BEGINNING WITH 00040H.
;PIC IS FULLY NESTED, NON-AUTO EOI.
;PIC IS IDENTIFIED AS SLAVE 0.
;USES-SETI, DESTROYS-AL.

          PUBLIC    INTSL

INTSL:    MOV       AL,11H           ;ICW1
          OUT       0C0H,AL
          MOV       AL,10H           ;ICW2
          OUT       0C2H,AL
          MOV       AL,00H           ;ICW3
          OUT       0C2H,AL
          MOV       AL,19H           ;ICW4
          OUT       0C2H,AL
          RET

          END
```

3-40. OPERATION

After initialization, the master PIC and slave PIC's can independently be programmed at any time by an Operation Command Word (OCW) for the following operations:

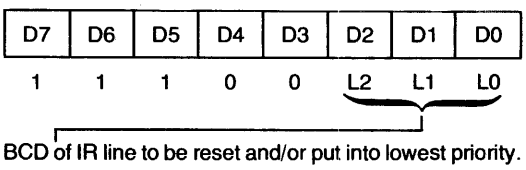
a. Auto-rotating priority.
b. Specific rotating priority.
c. Status read of Interrupt Request Register (IRR).
d. Status read of In-Service Register (ISR).
e. Interrupt mask bits are set, reset, or read.
f. Special mask mode set or reset.

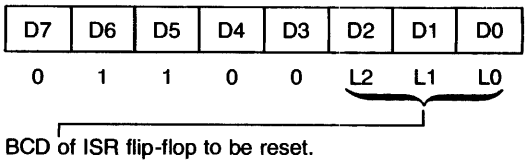
Table 3-28 lists details of the above operations. Note that an End-Of-Interrupt (EOI) or a Special End-Of-Interrupt (SEOI) command is required at the end of each interrupt service routine to reset the ISR. The EOI command is used in the fully nested and auto-rotating priority modes and the SEOI command, which specifies the bit to be reset, is used in the specific rotating priority mode. Tables 3-29 through 3-30 provide typical subroutines for the following:

a. Read IRR (table 3-29).
b. Read ISR (table 3-30).
c. Set mask register (table 3-31).
d. Read mask register (table 3-32).
e. Issue EOI command (table 3-33).

Table 3-28. PIC Operation Procedure

<table>
<tr><th>Operation</th><th>Procedure</th></tr>
<tr><td>Auto-Rotating Priority Mode</td><td>To set:
In OCW2, write a Rotate Priority at EOI command (A0H) to Port 00C0.

Terminate interrupt and rotate priority:
In OCW2, write EOI command (20H) to Port 00C0.</td></tr>
<tr><td>Specific Rotating Priority Mode</td><td>To set:
In OCW2, write a Rotate Priority at SEOI command in the following format to Port 00C0:
 

To terminate interrupt and rotate priority:
In OCW2, write an SEOI command in the following format to Port 00C0.
 

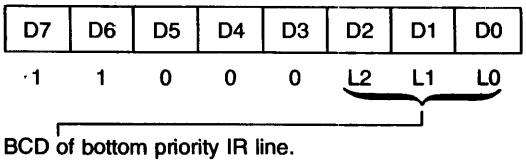
To rotate priority without EOI:
In OCW2, write a command word in the following format to Port 00C0:
 
</td></tr>
</table>

Table 3-28. PIC Operation Procedures (Continued)

<table>
<tr><th>Operation</th><th>Procedure</th></tr>
<tr><td>Interrupt Request Register (IRR) Status</td><td>The IRR stores a "1" in the associated bit for each IR input line that is requesting an interrupt. To read the IRR (refer to footnote):
(1) Write 0AH to Port 00C0.
(2) Read Port 00C0. Status is as follows:
<table><tr><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr><tr><td>IR Line:</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table></td></tr>
<tr><td>In-Service Register (ISR) Status</td><td>The ISR stores a "1" in the associated bit for priority inputs that are being serviced. The ISR is updated when an EOI command is issued. To read the ISR (refer to footnote):
(1) Write 0BH to Port 00C0.
(2) Read Port 00C0. Status is as follows:
<table><tr><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr><tr><td>IR Line:</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>Be sure to reset ISR bit at end-of-interrupt when in the following modes:
Auto-Rotating (both types) and Special Mask. To reset ISR in OCW2, write:
<table><tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>L2</td><td>L1</td><td>L0</td></tr></table>BCD identifies bit to be reset.</td></tr>
<tr><td>Interrupt Mask Register</td><td>To set mask bits in OCW1, write the following mask byte to Port 00C2:
<table><tr><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr><tr><td>IR Bit Mask:</td><td>M7</td><td>M6</td><td>M5</td><td>M4</td><td>M3</td><td>M2</td><td>M1</td><td>M0</td></tr></table>1 = Mask Set, 0 = Mask Reset
To read mask bits, read Port 00C2.</td></tr>
<tr><td>Special Mask Mode</td><td>The Special Mask Mode enables desired bits that have been previously masked; lower priority bits are also enabled.
To set, write 68H to Port 00C0.
To reset, write 48H to Port 00C0.</td></tr>
<tr><td colspan="2">NOTE:
If previous operation was addressed to same register, it is not necessary to rewrite the OCW.</td></tr>
</table>

Table 3-29. Typical PIC Interrupt Request Register Read Subroutine

```
;RR0 READS PIC INTERRUPT REQUEST REG.
;DESTROYS-AL.

            PUBLIC    RR0

RR0:        MOV       AL,0AH          ;OCW3 RR INSTRUCTION TO PIC
            OUT       0C0H,AL
            IN        AL,0C0H
            RET

            END
```

Table 3-30. Typical PIC In-Service Register Read Subroutine

```
;RIS0 READS PIC IN-SERVICE REGISTER.
;DESTROYS-A.

            PUBLIC    RIS0

RIS0:       MOV       AL,0BH          ;OCW3 RIS INSTRUCTION TO PIC
            OUT       0C0H,AL
            IN        AL,0C0H
            RET

            END
```

Table 3-31. Typical PIC Set Mask Register Subroutine

```
;SMASK STORES AL REG INTO PIC MASK REG.
;A ONE MASKS OUT AN INTERRUPT, A ZERO ENABLES IT.
;USES-AL, DESTROYS-NOTHING.

            PUBLIC    SMASK

SMASK:      OUT       0C2H,AL
            RET

            END
```

Table 3-32. Typical PIC Mask Register Read Subroutine

```
;RMASK READS PIC MASK REG INTO AL REG.
;DESTROYS-AL.

            PUBLIC    RMASK

RMASK:      IN        AL,0C2H
            RET

            END
```

Table 3-33. Typical PIC End-Of-Interrupt Command Subroutine

```
;EOI ISSUES END-OF-INTERRUPT TO PIC.
;DESTROYS-AL.

            PUBLIC    EOI

EOI:        MOV       AL,20H          ;NON-SPECIFIC EOI
            OUT       0C0H,AL
            RET

            END
```

3-41. 8086 INTERRUPT HANDLING

The 8086 CPU has two interrupt input request lines: Interrupt Request (INTR) and Non-Maskable Interrupt Request (NMI). All of the interrupt requests handled by the 8259A interrupt controller are connected to the INTR input. The NMI input on the iSBC 86/05 board is not used in the factory default configuration, but can be reconfigured for use with the parallel interface or iSBX Multimodule boards. Refer to Section 2-11 for complete jumper instructions.

Section 3-41 provides a summary of the NMI input functions and Section 3-42 summarizes INTR functions. For a complete discussion of 8086 interrupt handling, refer to *The 8086 Family User's Manual*, order number 9800722.

3-42. NON-MASKABLE INTERRUPT (NMI)

The NMI input has the higher priority of the two interrupt inputs. A low-to-high transition on the NMI input will be serviced at the end of the current instruction or between whole moves of a block type instruction. The worst case response to NMI is during a multiply, divide, or variable shift instruction.

When the NMI input is active, the CPU performs the following:

a. Pushes the flag registers into the stack (same as PUSHF).

b. Clears the Interrupt Flag (same as CLI). This disables all maskable interrupts.

c. Transfers control with an indirect call through vector location 00008.

The NMI input is intended mainly for catastrophic error handling, such as a system power failure interrupt. Upon completion of the service routine, the CPU automatically restores the flags and returns to the main program.

3-43. MASKABLE INTERRUPT (INTR)

The INTR input has the lower priority of the two interrupt inputs. A high level on the INTR input will be serviced at the end of the current instruction or at the end of a whole move for a block-type instruction.

When INTR goes active, the CPU performs the following (assuming the Interrupt Flag is set):

a. Issues two acknowledge signals; upon receipt of the second acknowledge signal, the interrupting device (master or slave PIC) will respond with a one-byte interrupt identifier.

b. Pushes the Flag registers onto the stack (same as a PUSHF instruction).

c. Clears the Interrupt Flag, thereby disabling further maskable interrupts.

d. Multiplies by four (4) the binary value (X) contained in the one-byte identifier from the interrupting device.

e. Transfers control with an indirect call through location 4X.

Upon completion of the service routine, the CPU automatically restores its flags and returns to the main program.

3-44. MASTER PIC BYTE IDENTIFIER. The master (on-board) PIC responds to the second acknowledge signal from the CPU only if the interrupt request from a non-slaved device; i.e., a device that is connected directly to one of the master PIC IR inputs. The master PIC has eight IR inputs numbered IR0 through IR7, which are identified by a 3-bit binary number. Thus, if an interrupt request occurs on IR5, the master PIC responds to the second acknowledge signal from the CPU by outputting the byte $00000101_2(05_H)$. The CPU multiplies this value by four and transfers control with an indirect call through $00010100_2(14_H)$.

3-45. SLAVE PIC BYTE IDENTIFIER. Each slave PIC is initialized with a 3-bit identifier (ID) in ICW3. These three bits will form a part of the byte identifier transferred to the CPU in response to the second acknowledge signal.

The slave PIC requests an interrupt by driving the associated master PIC IR line. The master PIC, in turn, drives the CPU INTR input high and the CPU outputs the first of two acknowledge signals. In response to the first acknowledge signal, the master PIC outputs a 3-bit binary code to slaved PIC's; this 3-bit code allows the appropriate slave PIC to respond to the second acknowledge signal from the CPU.

Assume that the slave PIC has the ID code 111_2 assigned in ICW3, and that the device requesting service is driving the IR2 line (010). Thus, in response to the second acknowledge signal, the slave PIC outputs 00111010_23A_H). The CPU multiplies this value by four and transfers control with an indirect call through $11101000_2(E8_H)$.

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a description of each major functional block on the iSBC 86/05 board. The purpose of the chapter is to show how the functional blocks interact during each mode of operation. The material in this chapter is intended to expand on the subject matter presented in the other chapters. This chapter does not provide detailed descriptions of the internal operation of each LSI device on the board.

4-2. FUNCTIONAL DESCRIPTION

Conceptually, the iSBC 86/05 board may be divided into nine major functional blocks:

CPU Section
On Board Memory
Interrupt Controller
Interval Timer Control
Parallel I/O Control
I/O & Memory Decode
iSBX Interface
Multibus Interface
Serial Communications Control

These functional blocks are shown in Figure 4-1, and are described in subsequent sections in this chapter. Other functions such as buffering, and the data and address buses are mentioned when appropriate throughout this chapter.

Intel Single Board Computer Signal Notation

Throughout this manual, and particularly in this chapter, various signals are referred to by their mnemonic terms. Some of these terms end with a slash (/). Table 4-1 outlines the signal notation for mnemonic terms ending with a slash and for those without the slash.

Table 4-1. Signal Notation

Function	Electrical	Logical	State
No Slash	High	1 True	Active, Asserted
	Low	0 False	Inactive
Slash	Low	1 True	Active, Asserted
	High	0 False	Inactive

Note: Electrical High is considered to be >2.0 V & < 5.25 V.
Electrical Low is considered to be <0.8 V & > -0.5 V.

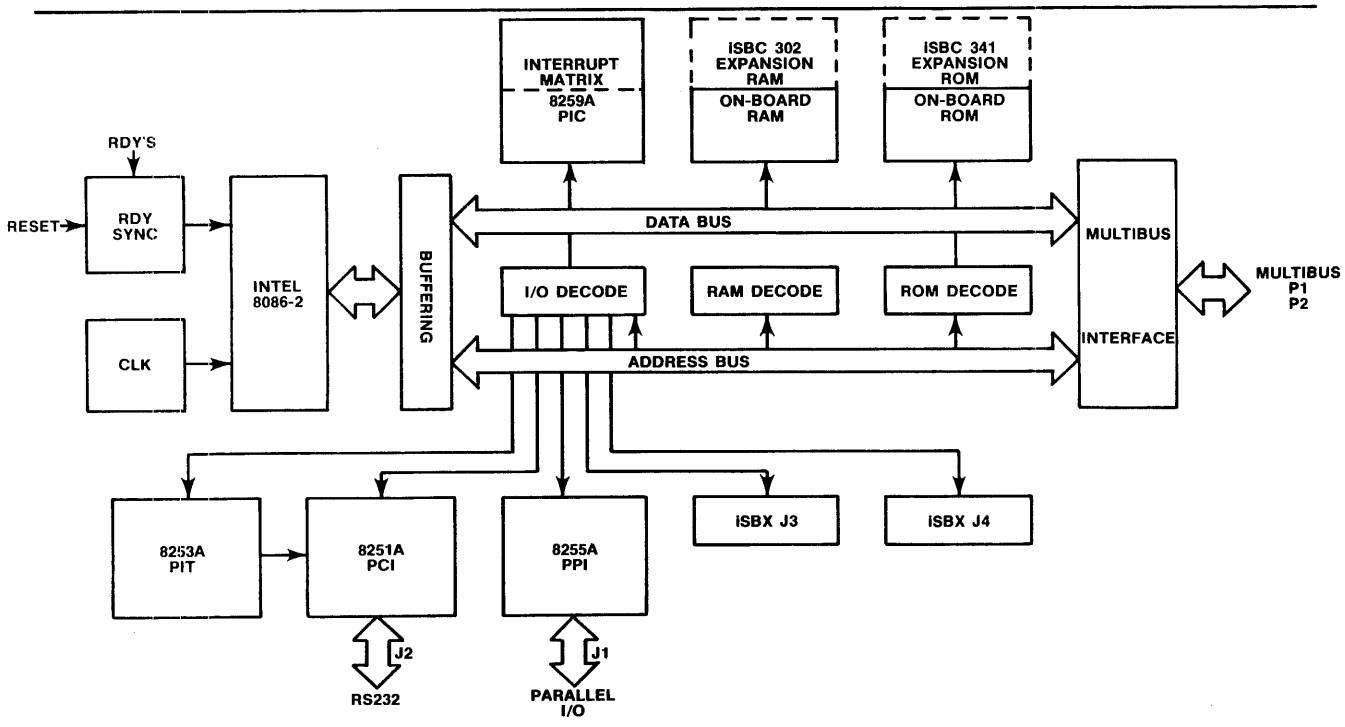


Figure 4-1. iSBC 86/05™ Simplified Block Diagram

4-3. CPU SECTION

The CPU section consists of the 8086-2 Microprocessor, the 8284A Clock Generator & Driver, the 8224 Clock Generator & Driver, and two 8288 Bus Controllers. The 8284A Clock Generator is used to supply the clock input to the microprocessor. This can be either 8 MHz or 5 MHz. The 8224 Clock Generator is used primarily to generate RESET and READY signals for the microprocessor, when the signal BOARD RESET/ is asserted.

4-4. 8086-2 MICROPROCESSOR. This device is internally divided into two processors, the Bus Interface Unit (BIU) and an Execution Unit (EU). The BIU is used to constantly monitor the EU and an internal queue for memory or I/O operations. Each time the BIU accesses the iSBC 86/05 internal bus, the 8086-2 processor must execute at least four major cycles, called T-States. The timing required for each T-State is discussed in the following sub-sections.

T1 State: The first T-State indicates the type of access and the location of the transfer participant. The processor first activates its status lines S0/, S1/, and S2/ indicating the type of operation to be performed for the bus cycle. When the status lines become active, the 8288 controller will activate its Address Latch Enable (ALE) signal, and enable the address buffers. When ALE is active, the address for the bus cycle is presented on the 8086-2 multiplexed address/data bus lines.

Before the end of T1, ALE goes inactive, and the address is latched. ALE is also inverted and used to clear the wait state generator. The ALE/ term is used to disable commands from the 8288 controller until the rising edge of T2. The only exception to this sequence occurs if the board is executing an Interrupt Acknowledge (INTA/) cycle. In this case, the MCE output of the 8288 controller becomes active with ALE, and is used to generate the INTA LOCK/ signal for the Multibus request action. The MCE signal will become inactive early in T2.

The following paragraphs briefly describe the relevant processor timing. Timing diagrams for T2, T3, and T4 are provided in Figures 4-2 and 4-3. Timing notation is given in Table 4-4 at the end of this chapter.

T2 State: During T2 the address presented during T1 is removed from the processor's address/data bus. There are three types of subsequent bus cycles during T2 following address removal: read sequence, write sequence, and halt or passive cycles.

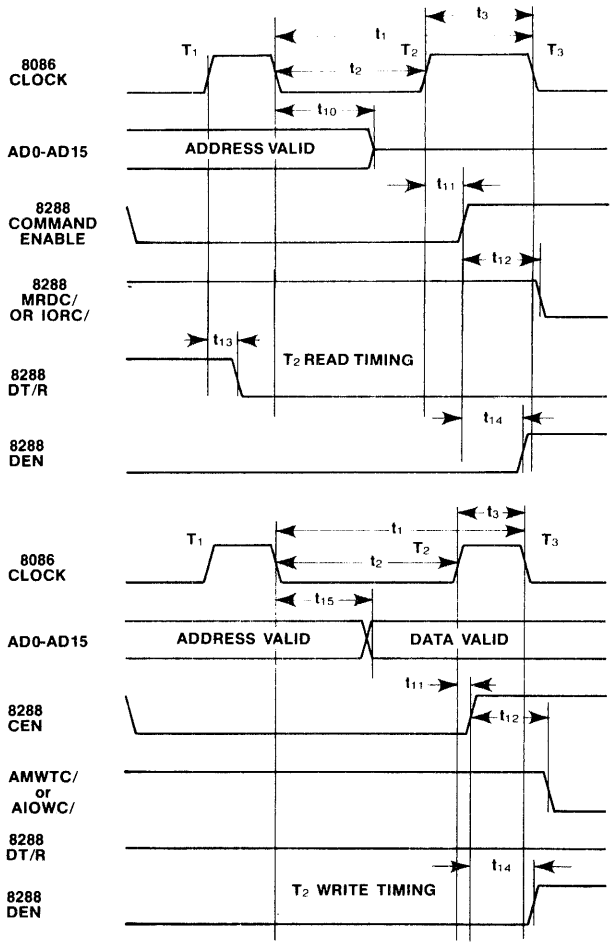


Figure 4-2. T2 Read and Write Timing

During a read, either MRDC/ or IORC/ becomes active. The processor removes its address from the bus, and sets the lines to the receive mode. The chip enable terms which come from the address, are generated if the address is a valid on-board location.

After the rising edge of the processor clock, the commands become active. The 8288 controller enables the data buffers, by setting the DT/R line low and the DEN line high, after the clock's rising edge.

During a write the processor drives the data lines. After the address is removed, the data is put on the multiplexed bus. The command, AMWTC/, and AIOWC/, and the chip enable terms become active as during a read cycle. The 8288 controller activates DEN for the transfer.

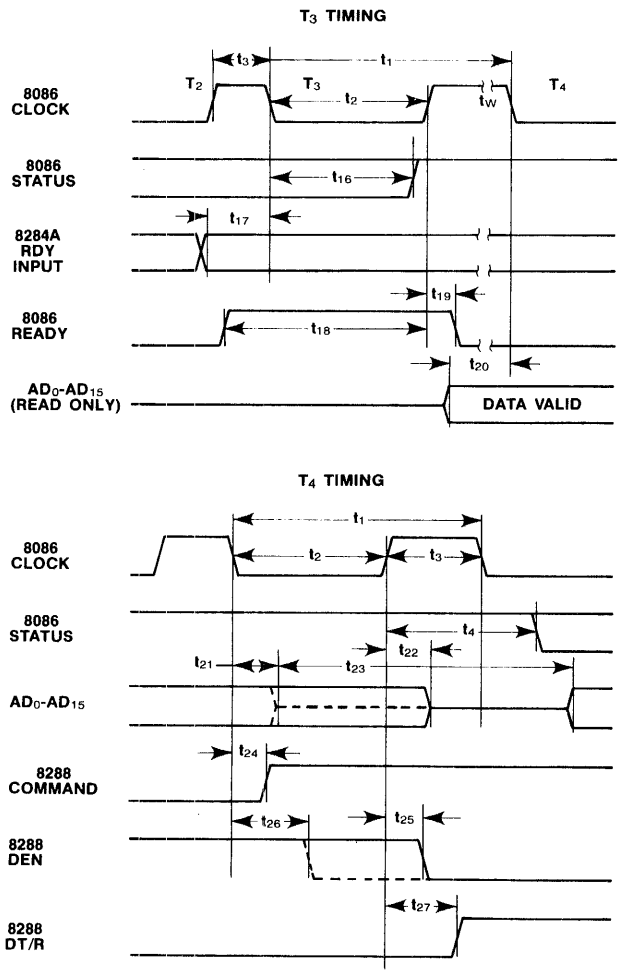


Figure 4-3. T3 and T4 Timing

If a HALT or PASSIVE state is indicated on the status lines, no commands will be issued. Chip enable terms will still be generated, though data integrity will be maintained.

T3 State: During this state, the data transfer is consummated if the access time of the peripheral device has been met. This mechanism is called acknowledge signalling, and is indicated by the READY signal to the 8284A device. If the peripheral does not send the acknowledge by the rising edge of the clock, the processor enters a WAIT State.

There are two sources for READY signals, one for on-board commands, which uses the wait state generator, and one for off-board using XACK/ and the bus timeout signals. When the processor receives the synchronized 8284A READY output, the status lines are forced to an inactive mode.

T4 State: During the T4 state all command lines are placed in their inactive mode. All control and direction lines also become inactive, until the processor status lines are asserted.

HOLD Sequences: A processor hold is initiated by pulsing the RQ/GT line. Typically this would only be done by a co-processor device such as the iSBC 337 Math Co-Processor device. The co-processor would pulse the RQ/GT line to obtain control of the local bus. The 8086-2 processor would then send a return pulse when it is ready to relinquish control of the local bus, and would place its address and data lines in the inactive state. When the co-processor is finished, it issues a third pulse which enables the 8086-2.

4-5. I/O AND MEMORY DECODE

When the processor issues an address, the I/O and memory decode circuitry must determine which device or memory location is being addressed. This decoding is done with two 3625A-1 bipolar, preprogrammed PROMs and associated support circuitry. The address must also be decoded to determine if a Multibus (off-board) transfer is required. One decode PROM is used for I/O addresses, and the other is used for memory addresses. They are discussed in Sections 4-6 and 4-7.

4-6. MEMORY DECODE PROM. The memory decode PROM accepts six address line inputs: A12 through A17. The PROM size jumper configuration is also used to indicate how much memory is actually on-board. (Jumper tables are in Chapter 2.) Two additional inputs to the decode circuitry indicate whether the optional iSBC 302 RAM Expansion Module is present (302 PRES/) and/or whether the optional iSBC 341 ROM Expansion Module is present (341 PRES/).

The page select demultiplexor is enabled by the MEM/IO cycle so that during I/O operations, the memory decode PROM outputs are inactive. The ALE input is used to prevent both decode PROMs from driving their output lines while the address and status is changing. The memory decode PROM outputs are pulled up and are therefore high when inactive. One of the outputs indicates if the address is on or off board (ON BD ADR/). The other three outputs are encoded to indicate the specific 16-bit bank of RAM or ROM to be enabled. Table 4-2 summarizes the output enabling signals.

4-7. I/O DECODE PROM. The I/O decode PROM is used to generate chip enable signals for the on-board I/O devices and the iSBX boards. Inputs to the decode PROM include address bits A3 through A7 and A0, MMPRES/, and two jumper select pins. The jumpers indicate whether iSBX boards are 8 or 16-bit devices (jumpers are described in Chapter 2).

Table 4-2. Memory Decode PROM Outputs

PROM OUTPUTS			Chip Enables
03	02	01	
0	0	0	PROM Bank 0
0	0	1	PROM Bank 1
0	1	0	PROM Bank 2 (iSBC 341)
0	1	1	PROM Bank 3 (iSBC 341)
1	0	0	RAM Bank 0
1	0	1	RAM Bank 1 (iSBC 302)
1	1	0	No Select
1	1	1	No Select

As with the memory decode PROM, the ALE signal is used to prevent contention on the OR tied PROM chip select. The other chip select is a NOR of address bits A8 through A15, and the MEM/IO cycle. This term is ANDed with INTA LOCK/ to prevent selecting the PROM during interrupt acknowledge sequences.

The output from pin 11 is used for the on-board/off-board signal (ON BD ADR). The other three outputs (01-03) are encoded to derive the appropriate chip enable terms. Table 4-3 summarizes this output encoding.

Table 4-3. I/O Decode PROM Outputs

I/O PROM OUTPUTS			Device Selected
03	02	01	
0	0	0	8251A
0	0	1	8253-5
0	1	0	8255A-5
0	1	1	8259A
1	0	0	SBX_1 CS_0
1	0	1	SBX_1 QCS_1
1	1	0	SBX_2 CS_0
1	1	1	SBX_2 QCS_2

4-8. MEMORY

iSBC 86/05 board memory consists of RAM and ROM/PROM/EPROM. These can be used in various addressing schemes. Refer to Tables 3-1 and 3-2 for addressing information. Four 28-pin ROM sockets are provided for using either 28-pin or 24-pin devices. Additional ROM memory is available with the optional iSBC 341 ROM Expansion Module. Jumpers are used to configure the board to the ROM size being used. These are defined in Chapter 2. The board's default configuration is for 2716 (2K X 8) devices.

Standard RAM consists of four 4K X 4 static devices. The amount of on-board RAM may be doubled to 16K bytes by installing the optional iSBC 302 RAM Expansion Module. A block diagram of the memory logic is shown in Figure 4-4.

RAM timing is provided in Figure 4-5, and ROM/PROM/EPROM timing is given in Figure 4-6. Timing notations are provided in Table 4-4 at the end of this chapter.

4-9. INTERVAL TIMER

The 8253A Programmable Interval Timer (PIT) includes three independently controlled counters which are used for on-board I/O and CPU interrupts. Each counter has its own input and output. Counter 0 is used as the CPU interrupt interval, connected to IR2 on the interrupt controller. It can also be used as an input to counter 1. Counter 1 can also be routed to the interrupt matrix or off-board via the parallel interface.

Counter 2 is used exclusively for the baud rate timer, clocking the serial interface controller. Refer to Chapter 2 for interval timer jumper information, and Chapter 3 for interval timer programming information.

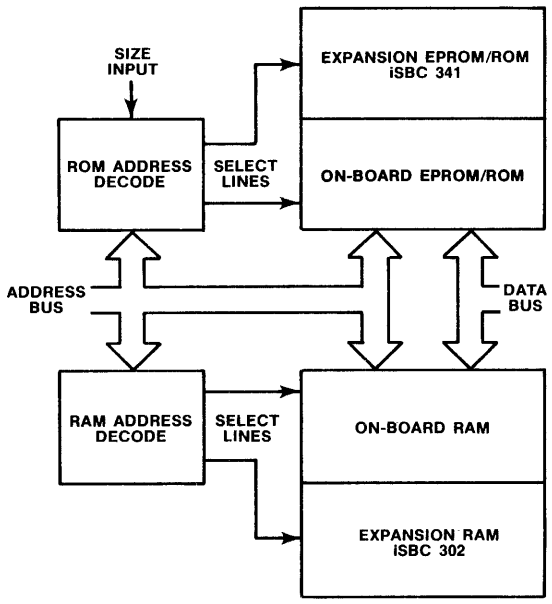


Figure 4-4. Memory Logic Block Diagram

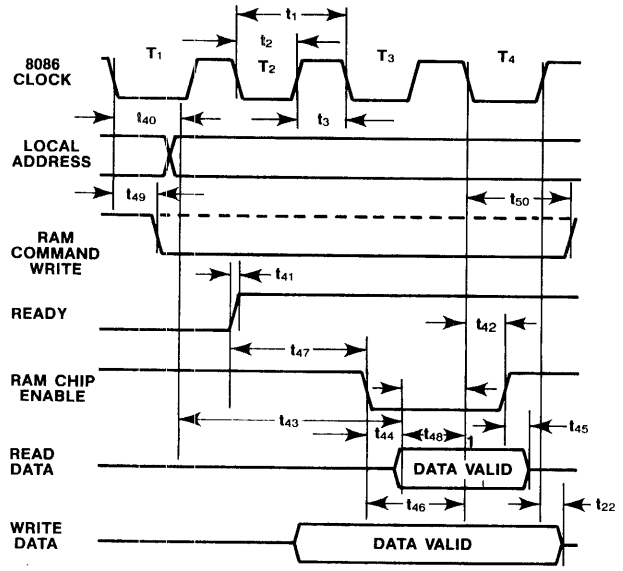


Figure 4-5. RAM Timing

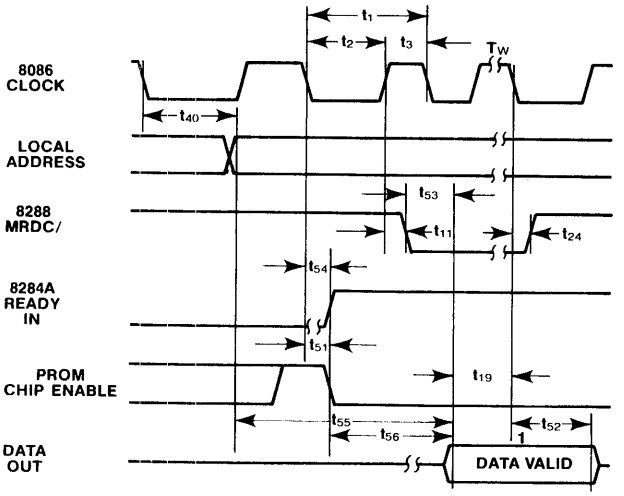


Figure 4-6. ROM Timing

4-10. SERIAL I/O

The 8251A Programmable Communications Interface (PCI) device provides RS 232C compatibility, and is configured with board jumpers as a data set. Synchronous or asynchronous mode, character size, parity bits, stop bits, and baud rates are all programmable (refer to Chapter 3). Data, clocks, and control lines to and from connector J2 are buffered with drivers and receivers. A second serial I/O channel may be derived by jumper connection, in conjunction with parallel port CC. Refer to Chapter 2 for jumper information.

4-11. PARALLEL I/O

A single 8255A Programmable Peripheral Interface (PPI) device provides 24 programmable I/O lines. A bus transceiver is used to interface port C8 to connector J1. Sockets are provided for the other two ports which will accommodate either line drivers or terminators. Ports CA and CC can be programmed as simple I/O ports or strobed I/O ports with handshaking. One port may be programmed as a bidirectional port with control lines. The iSBC 86/05 board includes many features which can be controlled by the parallel interface. Refer to Chapter 2 for these optional jumper configurations. Chapter 3 provides parallel port programming information and lists certain restrictions which apply in some modes of operation.

4-12. INTERRUPTS

All of the interrupt options are described in Section 2-16. The iSBC 86/05 board may respond to two basic types of interrupts, known as Multibus vectored and non-vectored interrupts. When either type of request is received by the on-board 8259A interrupt controller, an INTR is sent to the processor. If interrupts are enabled, the next bus cycle will be an interrupt acknowledge cycle. This causes INTA/ and MCE from the local 8288 controller to become active. When MCE becomes active, the INTA LOCK flip flop is set. If the Multibus Vectored Interrupt (BVI) disable jumper is not present (default), the Multibus lines will be requested during this cycle.

If the on-board PIC has been programmed to accept slave requests (refer to Chapter 3), a Multibus vectored interrupt will occur. The INTA LOCK/ signal disables on-board decoding, and generates the LOCK/ signal for the 8289 bus arbitration controller. During the second INTA/ cycle the interrupt controller DEN signal will remain inactive and a cascade PIC address will be placed on the multiplexed bus (AD8-AD10). A local READY signal is used to generate a READY for the first INTA/ cycle, but local READY signals are inhibited during the second INTA/ cycle. The second READY is generated by XACK/ from the Multibus lines. The wait state generator is used to provide the response time interval during a bus vectored interrupt sequence.

If the on-board PIC is not programmed for slave requests, a non bus vectored interrupt is generated. Jumpers provide two options for non bus vectored interrupt operation: no vectored interrupts and some vectored interrupts (refer to Chapter 2 for jumper information). If the jumpers are installed, the non bus vectored cycle will operate as a bus vectored one, except a local READY will be provided on the second INTA/ cycle.

Multibus vectored and non bus vectored interrupt timing are compared in Figures 4-7 and 4-8. Timing notation is given in Table 4-4 at the end of this chapter.

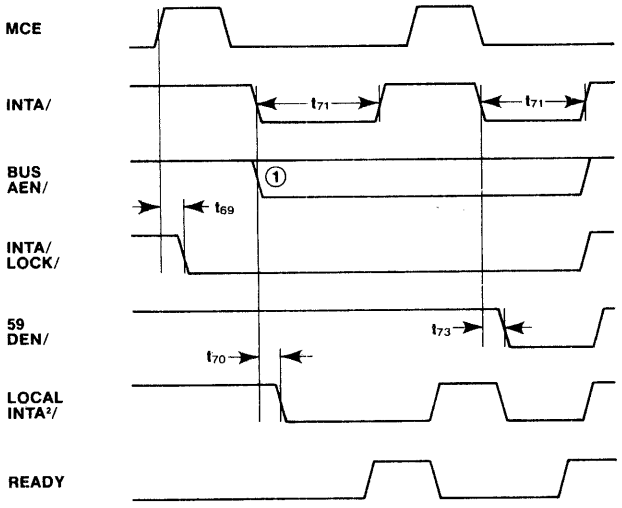


Figure 4-7. Interrupt Timing

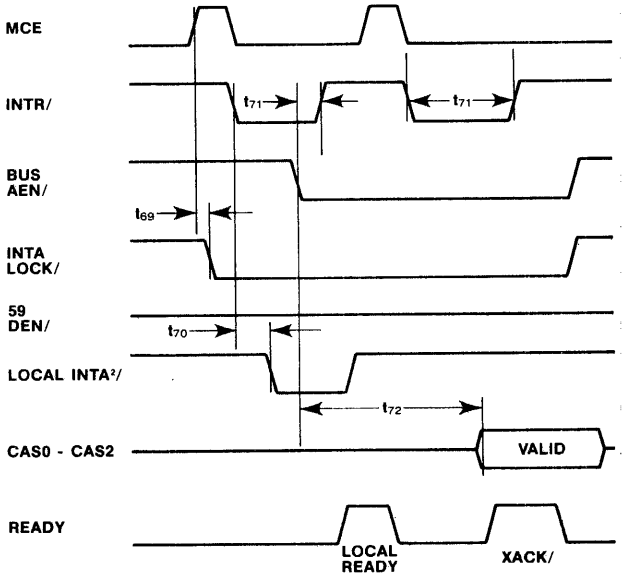


Figure 4-8. Multibus™ Vectored Interrupts

4-13. ON-BOARD I/O TIMING

On-board I/O timing is shown in Figure 4-9. Timing notation is provided in Table 4-4 at the end of this chapter.

4-14. MULTIBUS™ INTERFACE

This interface connects the iSBC 86/05 board to other boards in the system. The interface consists of address, data, and control lines, as shown in Table 2-15 (Chapter 2). Multibus circuitry consists of the 8289 Bus Arbiter device and several bus transceiver devices. Jumper options for the bus arbiter are given in Chapter 2.

The falling edge of BCLK/ provides the timing reference for the 8289 device, which allows the iSBC 86/05 board to assume the role of bus master. When the ON BD ADR/ signal is false, and the S0-S2 processor status signals indicate a read or write operation, the bus arbiter drives CBRQ/ and BREQ/ low and BPRO/ high. Refer to Figure 4-10.

The BREQ/ output, in conjunction with CBRQ/ from each bus master in the system is used by the Multibus interface when the bus priority is resolved by a parallel priority resolution scheme (refer to Section 2-27). If a serial priority resolution is used (Section 2-26), the BPRO/ output is used in conjunction with CBRQ/.

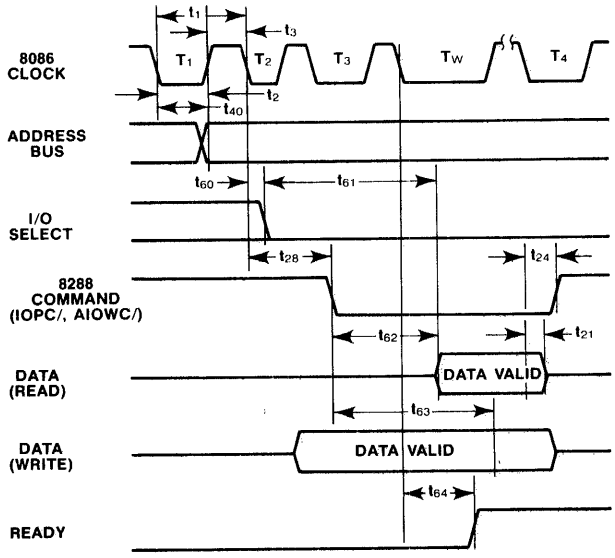


Figure 4-9. I/O Timing

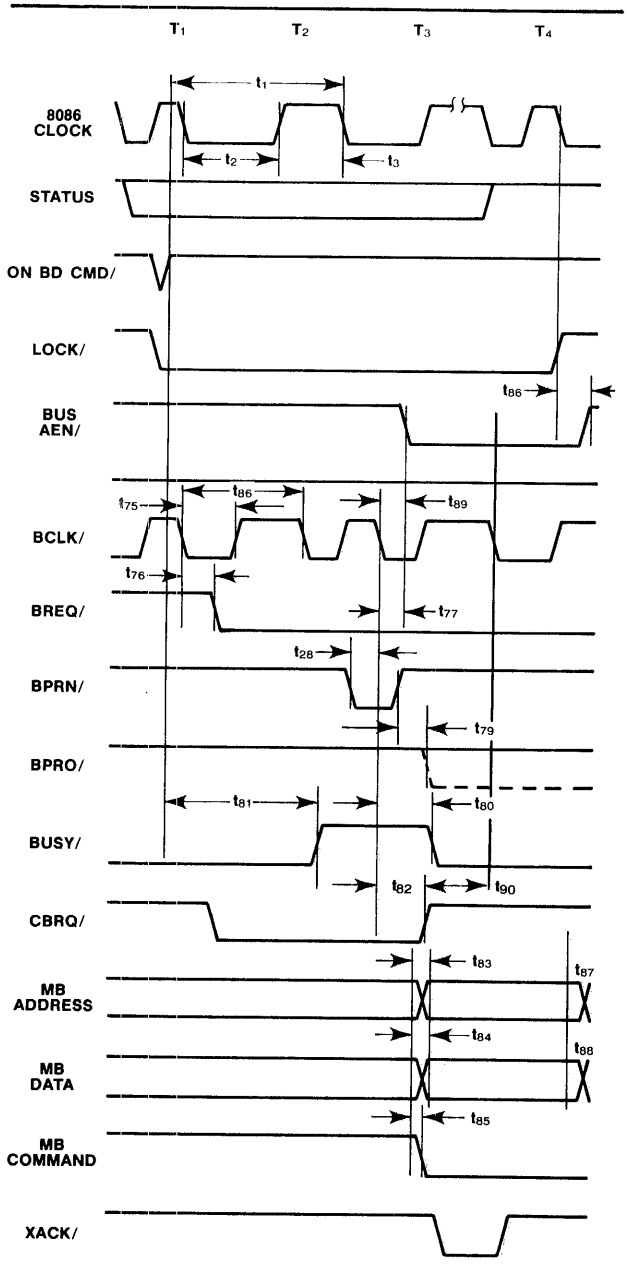


Figure 4-10. Multibus™ Exchange Timing

The iSBC 86/05 board gains control of the Multibus interface when the BPRN/ input to the bus arbiter is driven low and CBRQ/ is high. On the next falling edge of BCLK/, the bus arbiter drives BUSY/ and BUS AEN/ low. The BUSY/ output indicates the Multibus lines are in use and that the current bus master in control will not relinquish control until it raises its BUSY/ signal.

The BUS AEN/ output, which can be thought of as the bus master control signal, is applied to the processor clock generator, Multibus transceivers, and the local INTA/ circuitry. The negative true ON BD ADR/ signal enables the bus command decoder, which decodes the S0-S2 status lines from the processor. This will drive the appropriate command low (true) on the Multibus interface when CLK from the clock generator goes low. The bus controller also drives BUS DEN high to enable the bus transceiver. The transceiver's mode is determined by the state of DT/R output from the 8288 controller.

After the command is acknowledged the processor terminates the appropriate command. The bus arbiter terminates BUS AEN/ and the bus controller terminates BUS DEN. Depending on the board's jumper configuration, the bus arbiter will either retain or relinquish control of the Multibus lines.

The iSBC 86/05 board may invoke a LOCK condition on the Multibus lines, after it has gained control. This prevents the board from losing control of the Multibus lines. It prevents bus contention after a command has been executed. This is done with the 8086-2 processor via the instruction LOCK XCHG; or by setting the appropriate bit in an optional parallel port configuration (refer to Section 2-14). The LOCK condition is automatically asserted during an interrupt cycle.

4-15. iSBX™ MULTIMODULE INTERFACE

The iSBC 86/05 board is equipped with two iSBX Multimodule connectors (J3 and J4). iSBX signals and signal descriptions are given in Section 2-36. Multimodule boards are seen by the processor as on-board peripheral devices which require wait states. Multimodule circuitry is enabled by decoding the appropriate chip select signals (SBX1CS0-1 and SBX2CS0-1). These signals are decoded by the same I/O decoder used for other on-board I/O devices (refer to Section 4-7).

Timing for the iSBX bus is provided in Figure 4-11. Timing notation is provided in Table 4-4, at the end of this chapter.

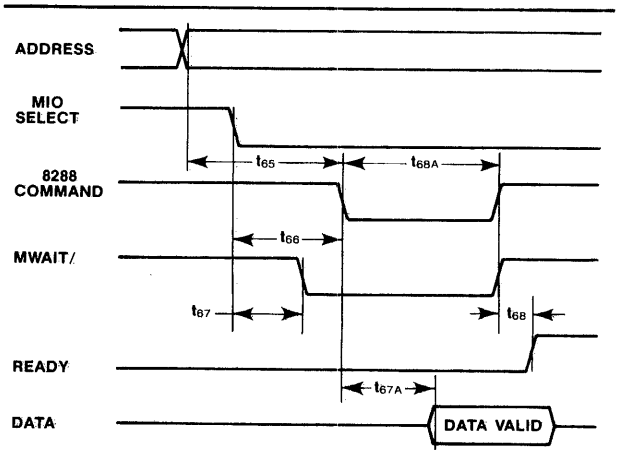


Figure 4-11. iSBX™ Bus Timing

Table 4-4. Timing Notation for Chapter 4 Diagram

		@ 5 MHz Min	@ 5 MHz Typ	@ 5 MHz Max	@ 8 MHz Min	@ 8 MHz Typ	@ 8 MHz Max
t_1	Clock Period		200			125	
t_2	Clock Low Time t_2 (min) = $\frac{2}{3}t_1$ -15 t_2 (max) = t_1-t_3 (min)	118		131	68		81
t_3	Clock High Time t_3 (min) = 1/3t_1+2 t_3 (max) = t_1-t_2 (min)	69		82	44		57
t_4	Status Active Delay	10		60	10		60
t_{10}	Address Float Delay	10		50	10		50
t_{11}	Clock to 8288 CEN t_{11} = 74S04 + t(74S112)			12			12
t_{121}	CEN to Command Active	10		35	10		35
t_{13}	Direction Control Active			50			50
t_{14}	CEN to DEN			20			20
t_{15}	Data Valid Delay	10		60	10		60
t_{16}	Status Inactive Delay	10		70	10		70
t_{17}	8284A Ready Setup	*		35	*		35
t_{18}	8086 Ready Setup t_{18} = t_2	118			68		
t_{19}	8086 Ready Hold	20			20		
t_{20}	8086 Data Setup	20			20		
t_{21}	8086 Data Hold on Read	10			10		
t_{22}	8086 Data Hold on Write	10			10		
t_{23}	Peripheral Data Inactive t_{23} = t_1-t_{21}+t_{15}	200		260	125		185
t_{24}	8288 Command Inactive Delay	10		35	10		35
t_{26}	8288 Control Inactive on Write	10		45	10		45
t_{26}	8288 Control Inactive on Read	10		45	10		45
t_{40}	Address Bus Valid t_{40} = t_5 + t(745373)			73			73
t_{41}	RAM Ready Delay t_{41} = t(74S00) + t(74S20)			20			20
t_{42}	RAM Enable Inactive t_{42} = t_{37}			21			21

Table 4-4. Timing Notation For Chapter 4 Diagram (Continued)

		@ 5 MHz Min	@ 5 MHz Typ	@ 5 MHz Max	@ 8 MHz Min	@ 8 MHz Typ	@ 8 MHz Max
t_{43}	RAM Address to Data $t_{43} = 3t_1-t_{40}-t_{20}$			507			262
t_{44}	RAM Enable Time $t_{44} = 2t_1-t_{47}-t_{20}$			194			94
t_{45}	RAM Disable Time $t_{45} = t_1+t_5-t_{12}-t_{42}$			154			79
t_{46}	Data Setup For RAM $t_{46} = 2t_1-t_{47}$			214			114
t_{47}	RAM Enable From T_2 $t_{47} = t_3+t_{11}+t_{12}$ + 2t(74S10) + t(74S139)			207			133
t_{48}	Data Buffer + Setup			20			20
t_{49}	RAM Write Active $t_{49} = t_1$ + t(74S373)			219			144
t_{50}	RAM Write Inactive $t_{50} = t_2+t_4$			191			141
t_{51}	PROM Enable from CLK $t_{51} = t_{35}-2$			16			16
t_{52}	Turn-off Time $t_{52} = t_1-t_{24}+t_5$			175			100
t_{53}	Turn-on Time $t_{53} = 2t_1-t_1-t_{11}+t_{19}$ $+nt_1$ n = # of waits			215 415 615 815			116 241 366 491
t_{54}	PROM Ready Delay t_{54} = 3t(74S00) + t(74S08) + (74S175)			44			44
t_{55}	PROM Address to Data Valid $t_{55} = 3t_15_{40}-t_{19}$ + nt_1			507 707 907 1107			282 407 532 657
t_{56}	PROM Enable to Data Valid $t_{56} = 2t_1-t_{51}-t_{19}$			364 564 764			216 341 466
t_{60}	I/O Select Delay t_{60} = t(74S138)-2			10			10
t_{61}	I/O Select Delay Enable $t_{61} = 2t_1-t_{60}-t_{48}+nt_1$			335 535 735 935			185 310 435 560

Table 4-4. Timing Notation For Chapter 4 Diagrams (Continued)

	@ 5 MHz Min	@ 5 MHz Typ	@ 5 MHz Max	@ 8 MHz Min	@ 8 MHz Typ	@ 8 MHz Max
t_{62} I/O Data From Command $t_{62} = 2t_1-t_{28}-t_{48}+nt_1$			210 410 610 810			60 185 310 435
t_{63} I/O Data Setup From Command $t_{63} = t_{62}+t_{48}$			265 465 665 865			115 240 365 490
t_{64} I/O Ready t_{64}=4 t(74S00) + t(74S08) + t(74S175)			37			37
t_{65} Address to Command $t_{65} = t_1-t_{40}+t_{28}$			261			136
t_{66} Enable to Command $t_{66} = t_{28}-t_{60}$			124			74
t_{67A} Command to Data $t_{67A} = Xt_1-t_{28}-t_{48}$ x=4a 8MHz 3 @ 8MHz -3a 5MHz 2 @ 5MHz			410			310
t_{67} MWAIT/ Active			70			70
t_{68A} SBC Command Width $t_{68A} = Xt_1-5_{28}+t_{24}$	475			375		
t_{68} Ready Active t_{68} = 4t(74S00) + t(74S175) + t(74S08)			42			42
t_{69} MCE to INTA LOCK/ t_{69} = t(74S74) + t(74LS74) t_{69} MCE to INTA LOCK/ t_{69} = **t(74S04) = t(74S112) t(74LS74)**			24			24
t_{70} INTA/ to INTA²/ t_{70} = t(74S74) + 2t(74S00)			19			19
t_{71} INTA/ Local Width $t_{71} = Xt_1-t_{12}+t_{24}$	410			260		
t_{72} INTA/ to CAS Valid			565			565
t_{73} INTA/ Bus Width	250			250		
t_{74} BCLK Clock Period	100			100		
t_{75} BCLK High Width	35		65	35		65
t_{76} BCLK to BREQ			35			35
t_{77} BCLK to BPRN			40			40
t_{78} BPRN to BCLK	15			15		
t_{79} BPRN to BPRO			25			25

Table 4-4. Timing Notation For Chapter 4 Diagrams (Continued)

	@ 5 MHz Min	Typ	Max	@ 8 MHz Min	Typ	Max
t_{80} BCLK to BUSY			60			60
t_{81} BUSY Setup to BCLK	20			20		
t_{82} BCLK to CBRQ			35			35
t_{83} Bus AEN/ to Address			15			15
t_{84} Bus AEN/ to Data			80			80
t_{85} Bus AEN/ to Command			40			40
t_{86} CLK to AEN/			65			65
t_{87} AEN/ to Address			15			15
t_{88} AEN/ to Data			80			80
t_{89} BCLK to AEN	40			40		
t_{90} CBRQ/ Setup to BCLK/	20			20		

Note: All times in nanoseconds.

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides the following service related information:

a. Repair assistance information.

b. Replacement parts list and diagram.

c. Jumper post location diagram.

d. Schematic diagrams.

5-2. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other MCSD products, it is usually stamped on a label.

c. Serial number of product. On boards, this number is usually stamped on the board. On other MCSD products, the serial number is usually stamped on a label.

d. Shipping and billing addresses.

e. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.

f. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following numbers for contacting the Intel Product Service Hotline:

Telephone:

All U.S. locations, except Alaska, Arizona & Hawaii:

(800) 528-0595

All other locations:

(602) 869-4600

TWX Number:

910 - 951 - 1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

5-3. REPLACEMENT PARTS

A complete list of replacement parts is provided in Table 5-1. This list provides the part number, manufacturer, description and quantity of the item. Notice that each item is referenced in the parts location diagram. Table 5-2 provides the full name of the manufacturer which is abbreviated in Table 5-1. Some of the parts are available from any normal commercial source, and should be ordered by their generic description. These items are called out as CML, rather than listing a specific part number. Figure 5-1 shows the location of each iSBC 86/05 referenced part in Table 5-1. Figures 5-4 and 5-6 show the location of the iSBC 341 ROM Expansion Module parts and the iSBC 302 RAM Expansion Module parts.

5-4. SERVICE DIAGRAMS

The following schematic diagrams are included in this chapter:

Figure 5-3 iSBC 86/05 Board

Figure 5-5 iSBC 341 ROM Expansion Module

Figure 5-7 iSBC 302 RAM Expansion Module

Notice that a functional description of each jumper connection on a particular schematic sheet is referenced to the left of the fold out sheet.

The schematic diagrams are current when the manual is printed. However, minor revisions to the diagrams may occur between manual printings. Therefore, Intel provides photocopies of the current

schematic diagrams with the board, when it is shipped from the factory. These diagrams should be inserted into this manual for future reference. In most instances, the diagrams shipped with the board will be identical to those printed in the manual.

5-5. INTERNAL SIGNALS

Internal board signals which traverse from one sheet to another in Figure 5-3 are identified by a single or double alpha character within a box (e.g., [G] [AN]). The signal mnemonic is shown adjacent to the boxed character, along with the source or destination sheet number. Signals coming into the sheet are shown on the left side of the diagram. Conversely, signals leaving the sheet are shown on the right side.

To follow a signal from one sheet to another, read the sheet number and boxed character, then look for the same boxed character on the indicated sheet. For example, if you are going to trace the path of MRDC/ when it exits sheet 4, the first step would be to turn to the indicated sheet. Since MRDC/ will be entering sheet 6, as indicated on sheet 4 look for the [BH] symbol on the left side of the sheet. Notice that the inputs on the sheet also list the source sheet number (sheet 4 in this example).

Each signal will keep the same boxed character throughout Figure 5-3. This will enable you to trace the signal to any sheet with minimal effort.

The internal board signal mnemonics are listed and defined in Table 5-3. The signals are listed according to boxed code alphabetical order.

Signals which do not have boxed codes are either board inputs or outputs. These signals are described in Chapter 2.

5-6. JUMPER LOCATIONS

Jumper post locations are shown in Figure 5-1. This drawing is provided for use as a quick reference in locating the physical location of a jumper post on the iSBC 86/05 board. Jumper locations are also listed on each schematic sheet, with a brief description of the jumper's function.

Table 5-1. iSBC 86/05™ Replacement Parts List

Reference Designator	Description	Mfr Part No.	Mfr Code	Qty
5-1	iSBC 86/05 Single Board Computer	142879-002	INTEL	1
C1-6, 8-11, 14, 16-31, 33-44, 49-50, 52, 57	Capacitor, cer. 0.1μf, 50V +80-20%	OBD	COML	43
C12, 15, 32	Capacitor mica 10pf, 500V 5%	OBD	COML	3
C13, 45, 46, 54, 55	Capacitor, cer. 10μf, 10V 20%	OBD	COML	5
C47	Capacitor, tant. 6.8μf, 35V 20%	OBD	COML	1
C53, 56	Capacitor, tant. 22μf, 15V, 10%	OBD	COML	2
CR1, 2	Diode, 1N 4148	OBD	COML	2
DS1	Diode, LED, red low profile	521-9180	DIALIGHT	1
J3, 4	iSBX connector, 44-pin	68-369	VIKING	2
J5, 6, 7	Socket (20-pin strip)	7195-295-5	EMC	1
R1, 10, 14, 17-19, 31, 32	Resistor, 10K ohm, ¼W, 5%	OBD	COML	8
R2	Resistor, 220K ohm, ¼W, 5%	OBD	COML	1
R3-5, 7, 12, 26	Resistor, 1K ohm, ¼W, 5%	OBD	COML	6
R6, 11, 13, 16, 25, 30	Resistor, 5.6K ohm, ¼W, 5%	OBD	COML	6
R8, 29	Resistor, 560 ohm, ¼W, 5%	OBD	COML	2
R9, 20	Resistor, 100K ohm, ¼W, 5%	OBD	COML	2
R33, 34	Resistor, 510 ohm, ¼W, 5%	OBD	COML	2
RP1	Resistor pack, 10K ohm, 6-pin, .75W 2%	OBD	COML	1
RP2	Resistor pack, 10k ohm, 10-pin, 1.25W 2%	OBD	COML	1
RP3	Resistor pack 1K ohm, 14-pin, 1.5W 2%	OBD	COML	1
U1, 18, 36	NAND gate, 2 input	74LS00	TI	3
U2, 28	AND gate, 2 input	74LS08	TI	2
U3, 55	OR gate, 2 input	74S32	TI	2
U4	Flip-flop, D-type	74S175	TI	1
U5	Multivibrator, mono. retrig.	74LS123	TI	1
U6	Inverter	74LS04	TI	1
U7, 49, 64, 65	Bus Transceiver	8287	INTEL	4
U12	Counter, sync. 4-bit	74S163	TI	1
U13	Counter, sync. 4-bit	74LS163	TI	1
U14	Line Receiver	75188N	TI	1
U15	Line Receiver	75189AN	TI	1
U16, 17	Clock Generator/Driver	8224	INTEL	2
U19, 39	NAND gate, 3 input	74S10	TI	2
U20	Flip-flop, D-type	74LS74	TI	1
U21	Prog Interrupt Controller	8259A	INTEL	1
U22	Prog Peripheral Inteface	8255A-5	INTEL	1
U23	Prog Interval Timer	8253-5	INTEL	1
U24	Prog Comm. Interface	8251A	INTEL	1
U25, 48	Bus Transceiver	8286	INTEL	2
U26, 41	Decoder, 3 to 8	74S138	TI	2
U27	NOR gate, 2 input	74S02	TI	1
U29, 38	Inverter	74S04	TI	2
U30, 50	NAND gate, 2 input	74LS00	TI	2
U31	Bus Driver	DM8097N	NSC	1
U32	Microprocessor, 16-bit	8086-2	INTEL	1
U36	NOR gate, 5 input	74S260	TI	1
U40, 54	Decoder, 2 to 4	74S139	TI	2

Table 5-1. iSBC 86/05™ Replacement Parts List (Continued)

Reference Designator	Description	Mfr Part No.	Mfr Code	Qty
U42	Inverter, OC High Voltage	7406	TI	1
U43	Flip-Flop, JK, Neg. Edge Trig.	74S112	TI	1
U44, 59	Bus Controller	8288	INTEL	2
U45	Clock Generator & Driver	8284A	INTEL	1
U46, 51, 68	Latch, D-type	74S373	TI	3
U47, 56, 74	AND gate, 2 input	74S08	TI	3
U52, 53, 70, 71	RAM, static 4K x 4	2168R	INTEL	4
U57	NAND buffer, 2 input	74S37	TI	1
U58	Bus Arbiter	8289	INTEL	1
U60, 62, 63	Buffer/Driver/Receiver	74S240	TI	3
U61	Buffer/Driver/Receiver	74LS240	TI	1
U72	Pre-programmed PROM (I/O)	143635-001	INTEL	1
U73	Pre-programmed PROM (Memory)	143636-001	INTEL	1
XU7	Socket, 20-pin DIP	DILB20P-108	BURNDY	1
XU8-11	Socket, 14-pin DIP	DILB14P-108	BURNDY	4
XU32	Socket, 40-pin DIP	540-AG11D	AUGAT	1
XU33, 34, 66, 67	Socket, 28-pin DIP	528-AG37D	AUGAT	4
XU35	Socket, 14-pin DIP	514-AG37D	AUGAT	1
XU52, 53, 70, 71	Socket, 20-pin DIP	520-AG37D	AUGAT	2
Y1	Crystal, 19.6608 MHz	OBD	CRYSTEK	1
Y2	Crystal, 15 MHz	M15A	CRYSTEK	1
U3	Crystal, 24 MHz	OBD	CRYSTEK	1
—	Plug, shorting, 2 position	530153-2	AMP	30
—	Plug, shorting, U35	8136-475G1	AUGAT	3

Table 5-2. Manufacturers Names

Mfr. Code	Manufacturer
AMP	AMP Incorporated
AUGAT	Augat Incorporated
BURNDY	Burndy Corporation
CRYSTEK	Crystek Crystals Corporation
DIALIGHT	Dialight Corporation
EMC	EMC Controls Incorporated
NSC	National Semiconductor Corporation
TI	Texas Instruments Incorporated
VIKING	Viking Connectors Incorporated

NOTE: OBD = Order by description;
CML = Any commercial source

Table 5-3. List of Internal Signal Mnemonics

Code	Mnemonic	Description
A	BUS AEN/	Bus address enable
B	Not Used	
C	Not Used	
D	ON BD ADR/	On-board address
E	INTA LOCK/	Interrupt acknowledge lock
F	TEST/	Test input to 8086, from parallel interface
G	INTR	Interrupt request input to 8086
H	NMI	Non-maskable input to 8086
I	RST/	Inverted RESET
J	RST	RESET
K	LOCK/	Bus lock from 8086
L	BHE/S7/	Local bus high/status bit 7 output from 8086
M	A19/S6	Address/status bit output from 8086
N	A18/S5/	Address/status bit output from 8086
O	A17/S4	Address/status bit output from 8086
P	A16/S3	Address/status bit output from 8086
Q	AD0-AD15	Internal data/address bus lines
R	S2/	Status bit output from 8086
S	S1/	Status bit output from 8086
T	S0/	Status bit output from 8086
U	ALE	Address latch enable output from 8086
V	BHE/	Local bus high enable
W	A0-A19	Internal extended address bus lines
X	W/R	Write enable signal to RAM array
Y	MEM/IO	Memory or I/O selector
Z	D0-D7	Low byte data lines
AA	Not Used	
AB	Not Used	
AC	DEN	Data enable bit from 8288
AD	SYS CLK/	Inverted 8MHz on-board clock from 8284
AE	MMPRES/	Multimodule board present indicator
AF	CLK	8MHz on-board clock from 8284
AG	RAM0 HIGH/	RAM array 0 high byte enable
AH	RAM1 HIGH/	RAM array 1 high byte enable
AI	RAM0 LOW/	RAM array 0 low byte enable
AJ	RAM1 LOW/	RAM array 1 low byte enable
AK	PROM 0 LOW/	PROM array 0 low byte enable
AL	PROM 1 LOW/	PROM array 1 low byte enable
AM	PROM 2 LOW/	PROM array 2 low byte enable
AN	PROM 3 LOW/	PROM array 3 low byte enable
AO	PROM 0 HIGH/	PROM array 0 high byte enable
AP	PROM 1 HIGH/	PROM array 1 high byte enable
AQ	PROM 2 HIGH/	PROM array 2 high byte enable
AR	PROM 3 HIGH/	PROM array 3 high byte enable
AS	8251A CS/	PCI (USART) chip select
AT	8253A CS/	PIT (Interval Timer) chip select
AU	8255A CS/	PPI (Parallel Port) chip select
AV	8259A CS/	PIC (Interrupt Controller) chip select
AW	SBX2 CS0/	Multimodule 1, chip select 0
AX	SBX2 UCS1/	Unqualified chip select 1
AY	SBX1 CS0/	Multimodule 1, chip select 0
AZ	SBX1 UCS1/	Unqualified chip select 1
BA	BCLK	Multibus clock
BB	OVERRIDE/	Multibus override
BC	MCLK/	iSBX Multimodule clock (same as BCLK/)
BD	Not Used	
BE	INTA/	Interrupt Acknowledge
BF	IORC/	I/O Read Command from 8288
BG	AIOWC/	Advanced I/O write command from 8288
BH	MRDC/	Memory read command from 8288
BI	AMWTC/	Advanced memory write command from 8288
BJ	DT/R	Data transmit/receive signal from 8288
BK	ALE/	Address Latch Enable from 8288
BL	Not Used	
BM	Not Used	
BN	PU1	Pull-up resistor
BO	INTA LOCK	Interrupt acknowledge lock

Table 5-3. iSBC 86/05 Internal Signal Mnemonics (Continued)

Code	Mnemonic	Description
BP	59 INTA/	Interrupt acknowledge from PIC
BQ	LOCAL INTA2	Local interrupt acknowledge
BR	MWAIT2/	iSBX Multimodule 2 wait signal
BS	MWAIT1/	iSBX Multimodule 1 wait signal
BT	RAM/PROM	RAM or PROM select from memory decode
BU	BUSY/	Memory busy
BV	RDY/	Memory ready
BW	Not Used	
BX	EXT CLK/	External (off-board) clock for PIT
BY	GATE0 CNTRL	Gate 0 line for PIT
BZ	GATE1 CNTRL	Gate 1 line for PIT
CA	STXD	Secondary Transmit data output
CB	SITX	Serial Interface Transmit Interrupt
CC	SIRX	Serial Interface Receive Interrupt
CD	Not Used	
CE	TIMER0 INTR	PIT output 0 to PIC
CF	TIMER1 INTR	PIT output 1 to PIC
CG	PA INTR	Parallel port "A" interrupt to PIC
CH	CB INTR	Parallel port "B" interrupt to PIC
CI	BUS INTR OUT	Multibus interrupt output
CJ	NMI MASK/	Non-maskable interrupt mask
CK	SBX2 INT0	Multimodule 2, interrupt 0
CL	SBX2 INT1	Multimodule 2, interrupt 1
CM	SBX1 INT0	Multimodule 1, interrupt 0
CN	SBX1 INT1	Multimodule 1, interrupt 1
CO	59 DEN/	Data bus enable from PIC
SS/	PLC	Power Line Clock from power supply
UU	PU2	Pull-up resistor number 2
XX	I/O CS/	I/O data bus enable
ZY	BUS INTA/	Multibus interrupt acknowledge
ZZ	BUS LOCK/	Multibus lock

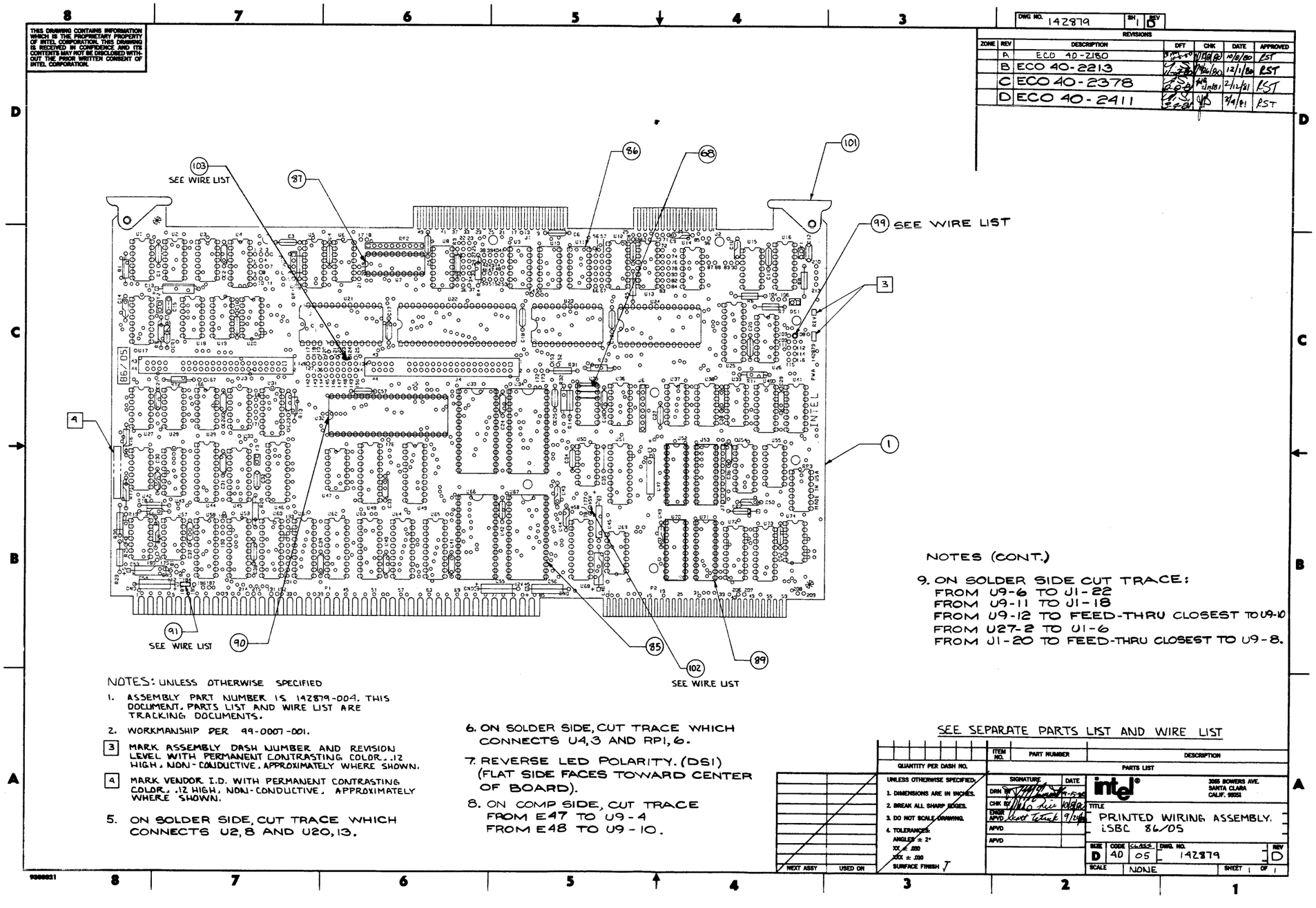


Figure 5-1. iSBC 86/05™ Board Parts Location Drawing

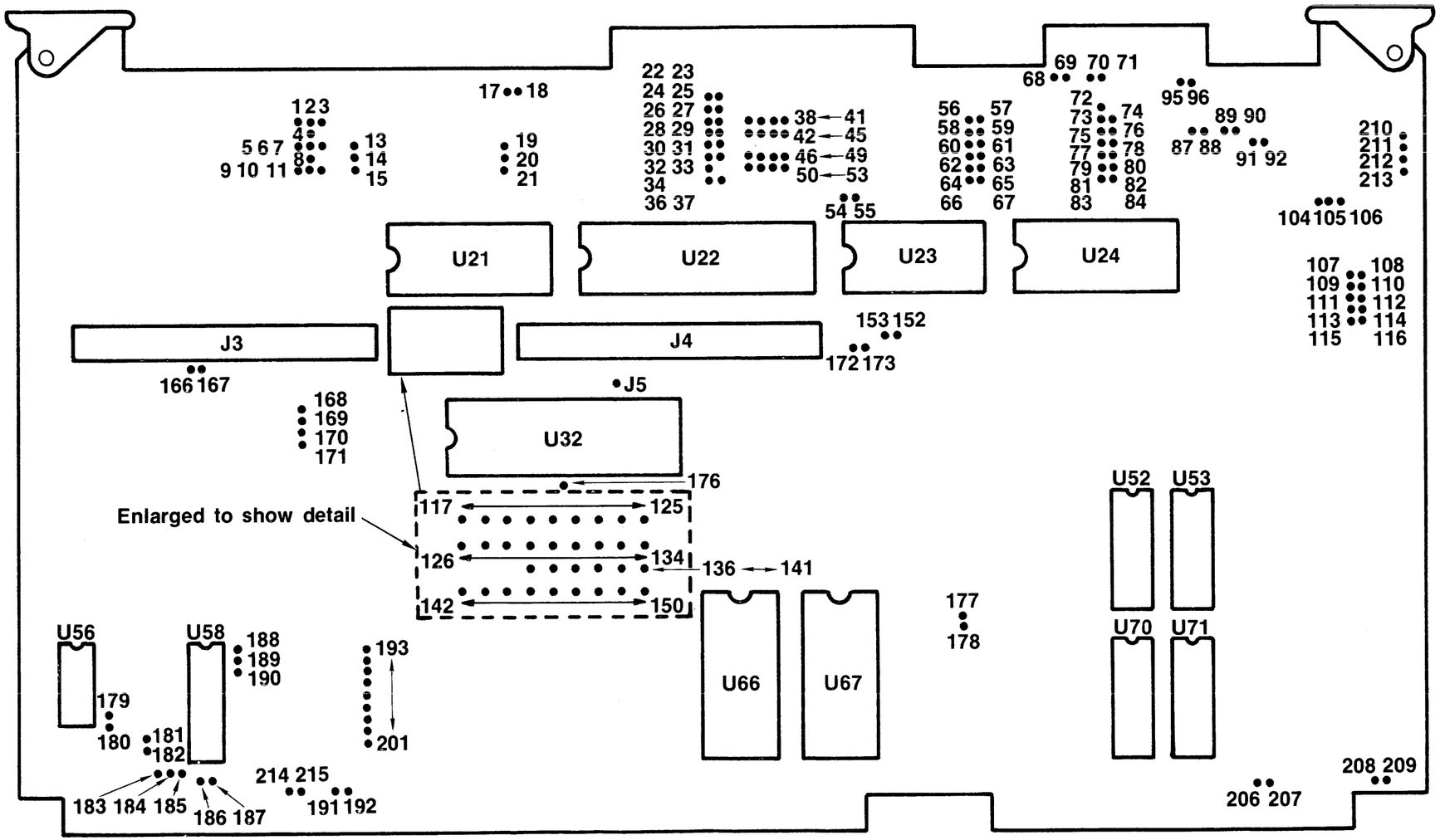


Figure 5-2. iSBC 86/05™ Board Jumper Post Location Drawing

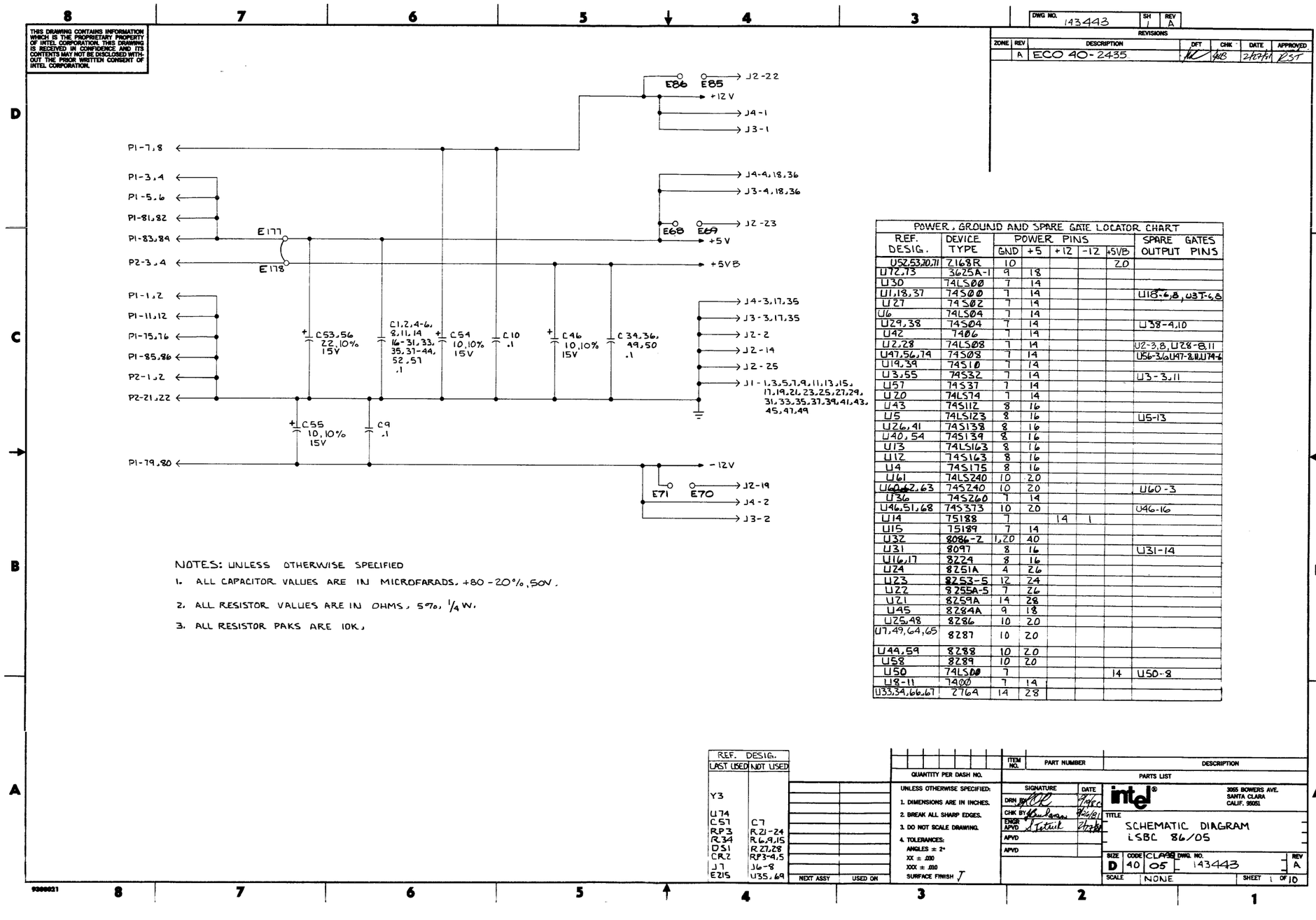


Figure 5-3. iSBC 86/05™ Board Schematic Diagram (Sheet 1 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

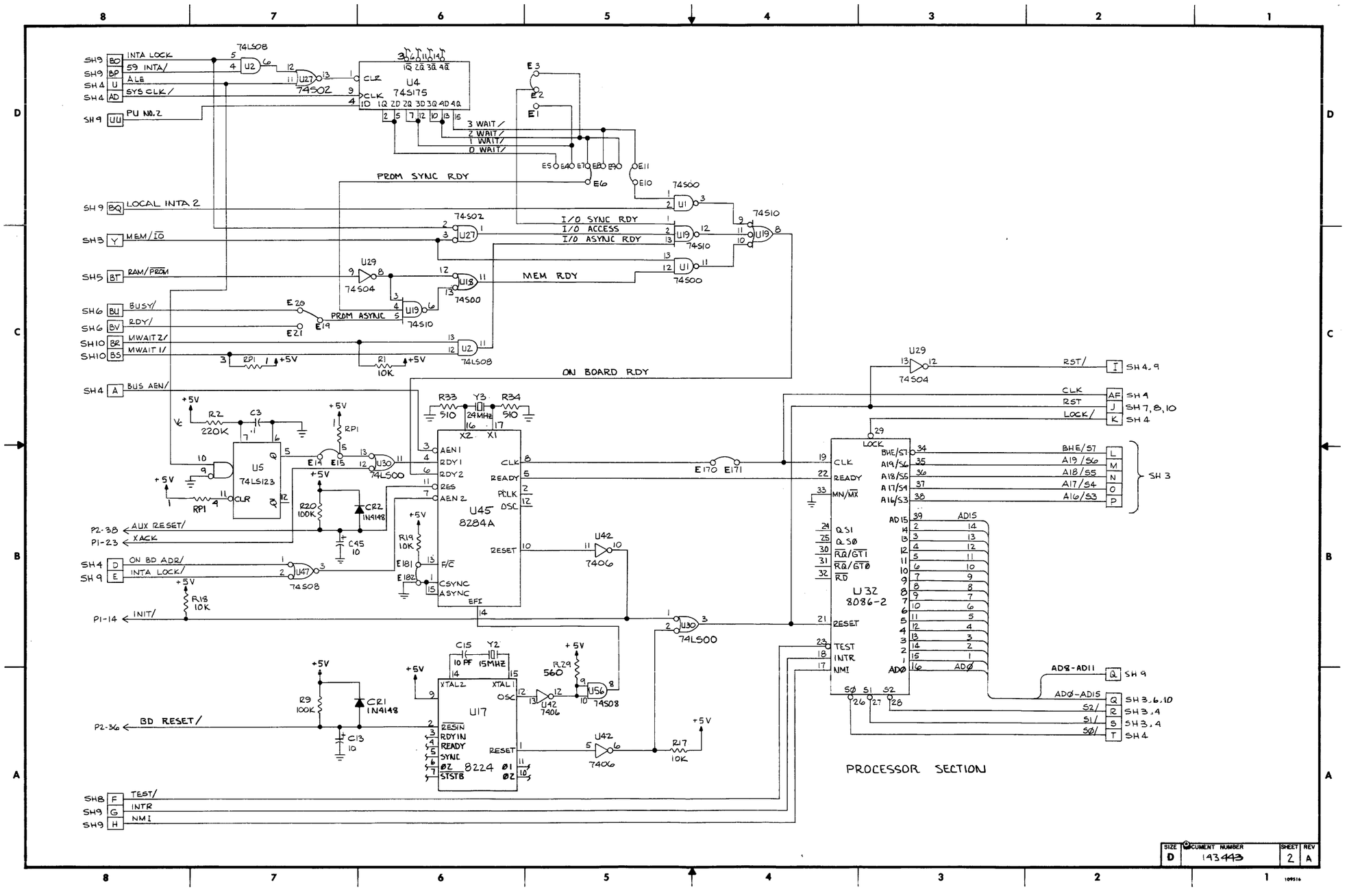
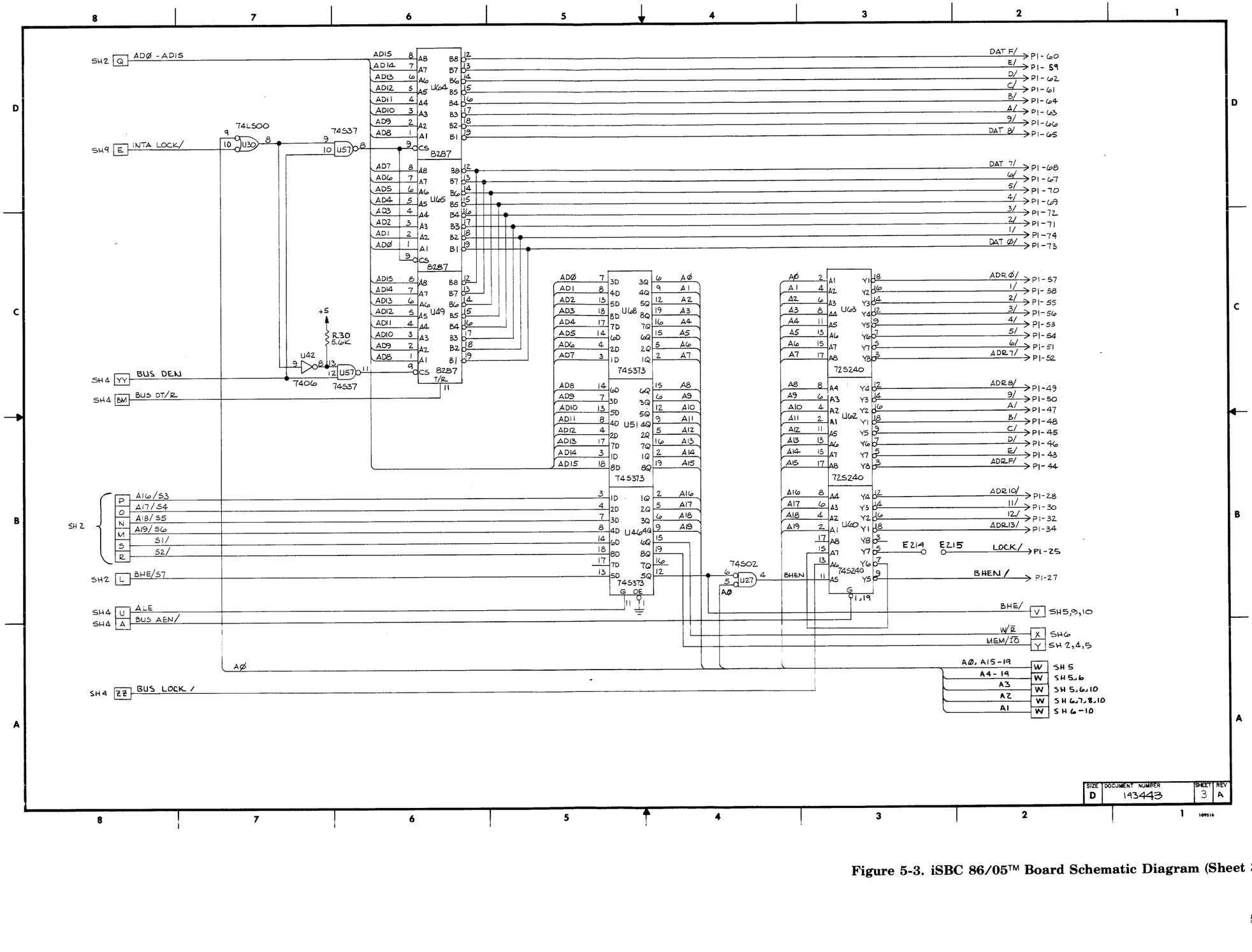


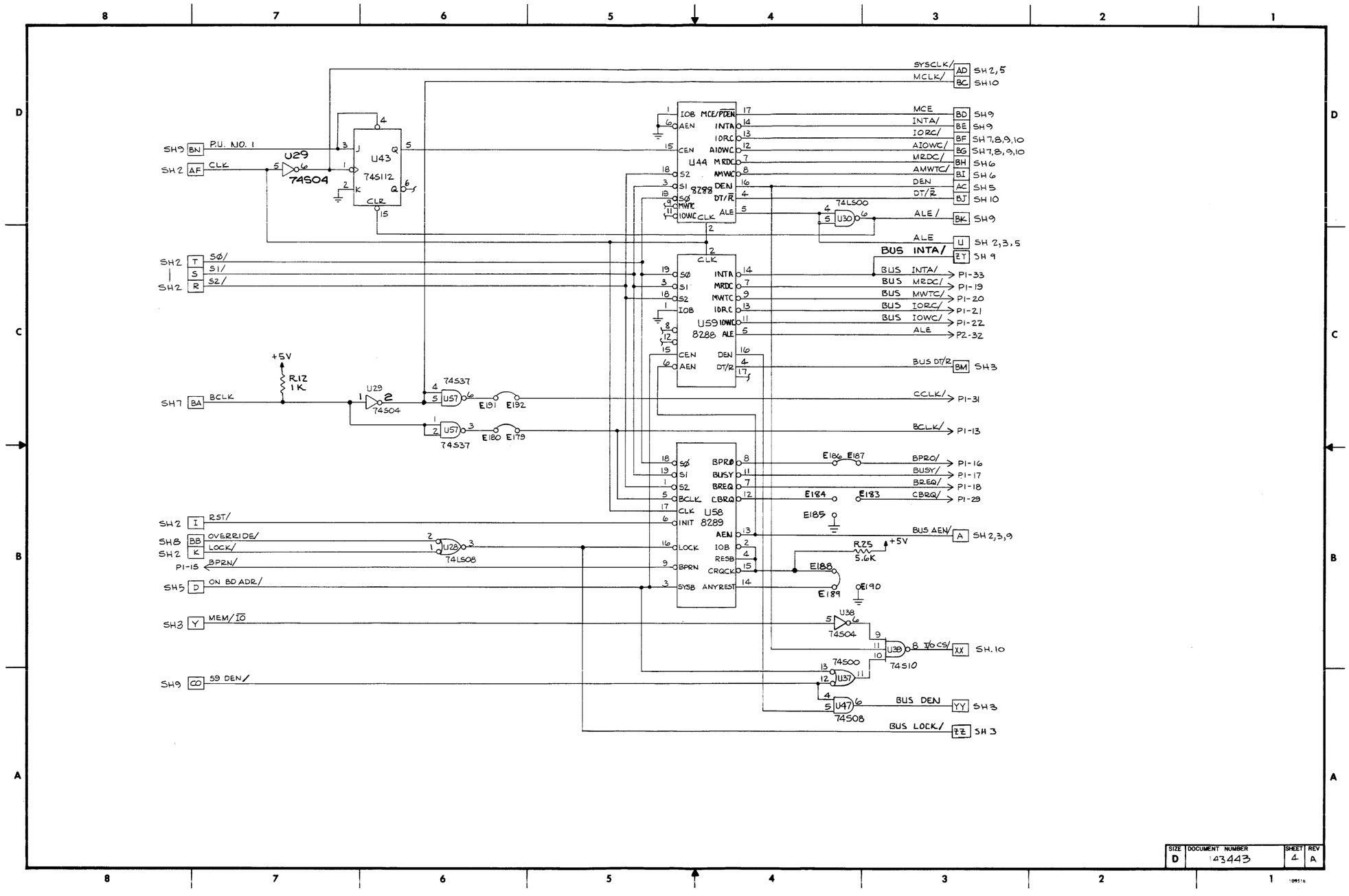
Figure 5-3. iSBC 86/05™ Board Schematic Diagram (Sheet 2 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.



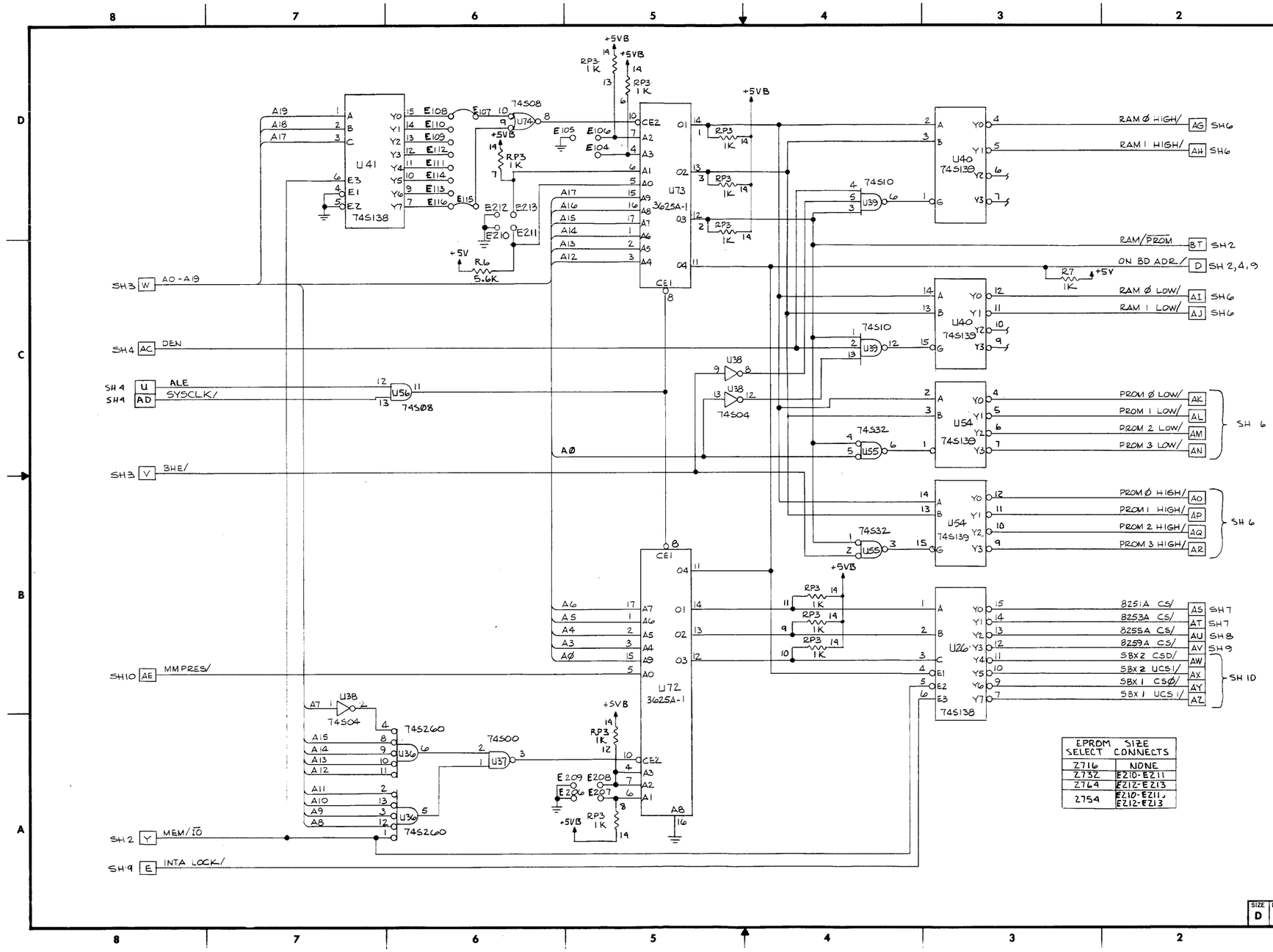
CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-3. iSBC 86/05™ Board Schematic Diagram (Sheet 3 of 10)



CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-3. iSBC 86/05™ Board Schematic Diagram (Sheet 4 of 10)



EPROM SELECT	SIZE CONNECTS
2716	NONE
2732	E210-E211
2764	E212-E213
2754	E210-E211, E212-E213

SIZE	DOCUMENT NUMBER	SHEET	REV
D	143443	5	A

Figure 5-3. iSBC 86/05™ Board Schematic Diagram (Sheet 5 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

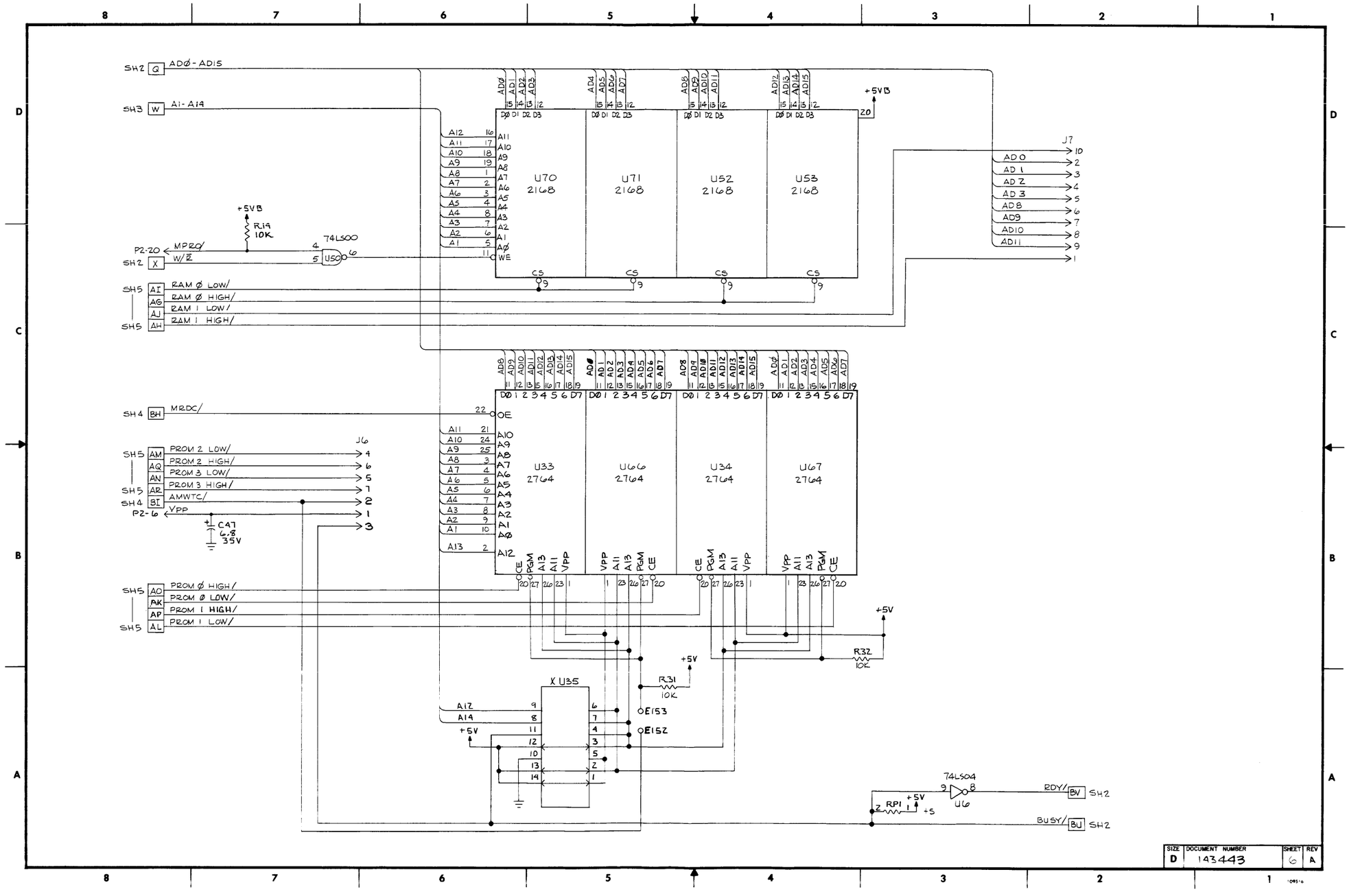


Figure 5-3. iSBC 86/05™ Board Schematic Diagram (Sheet 6 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

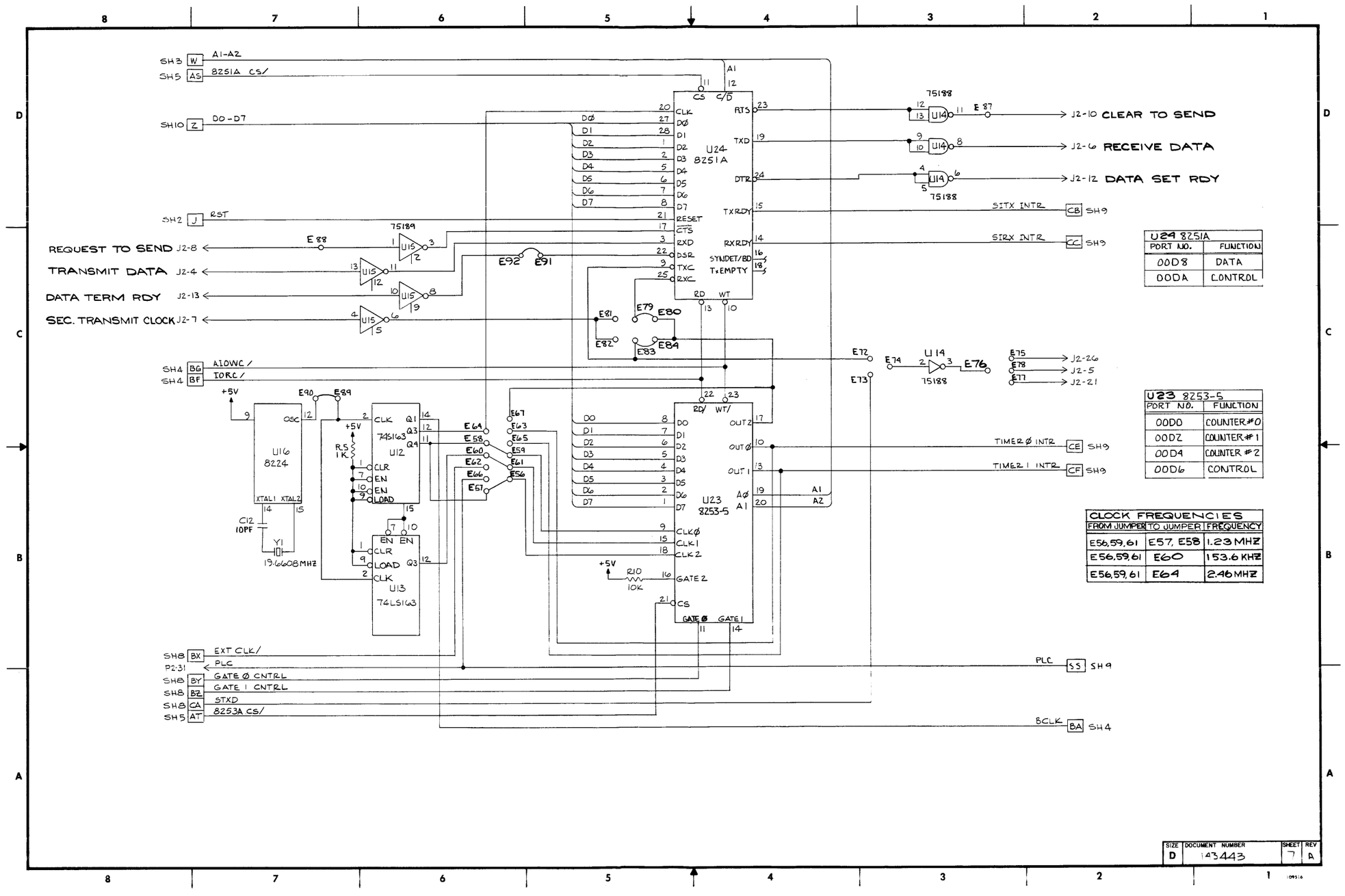


Figure 5-3. iSBC 86/05™ Board Schematic Diagram (Sheet 7 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

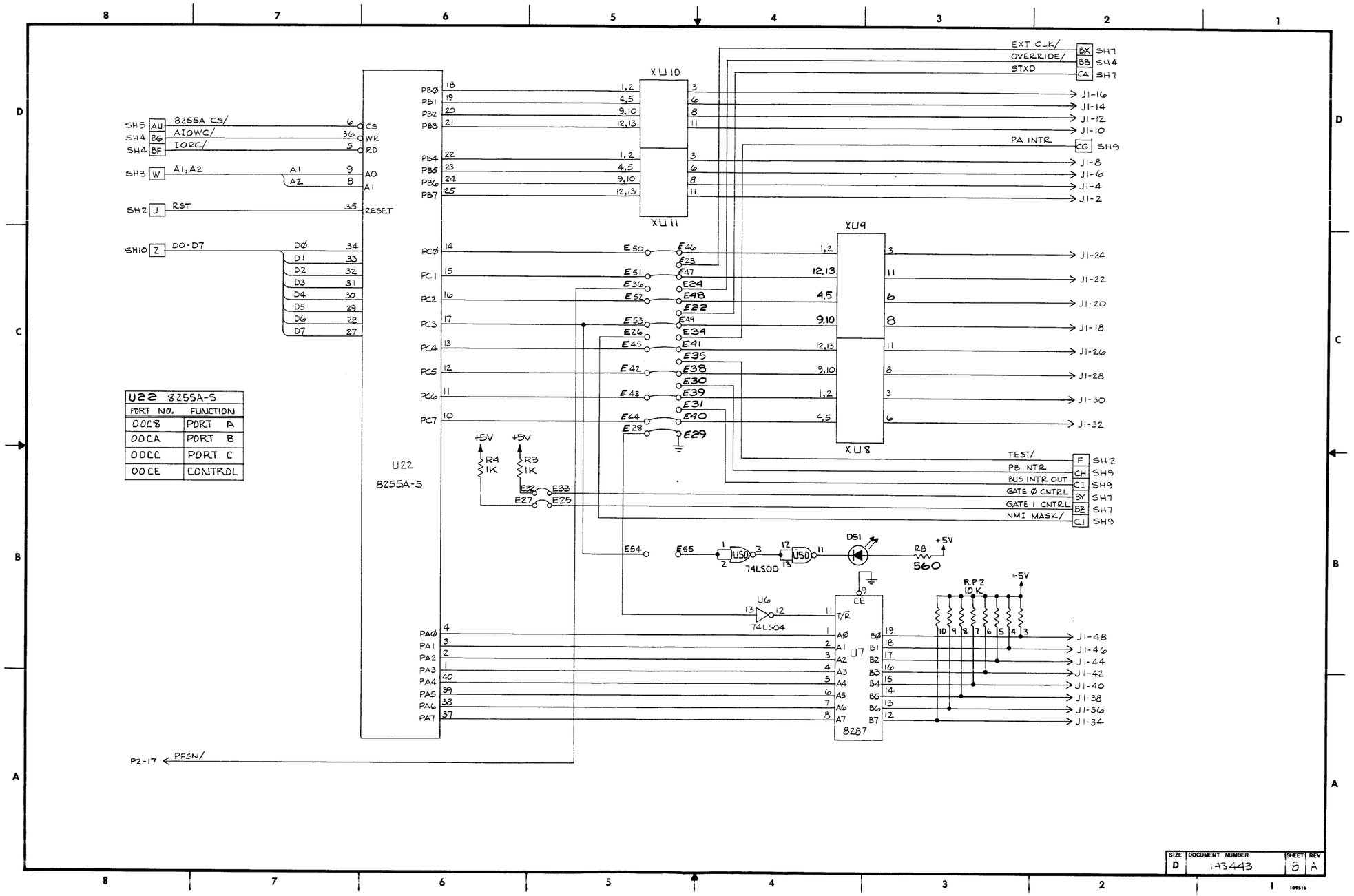


Figure 5-3. iSBC 86/05™ Board Schematic Diagram (Sheet 8 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

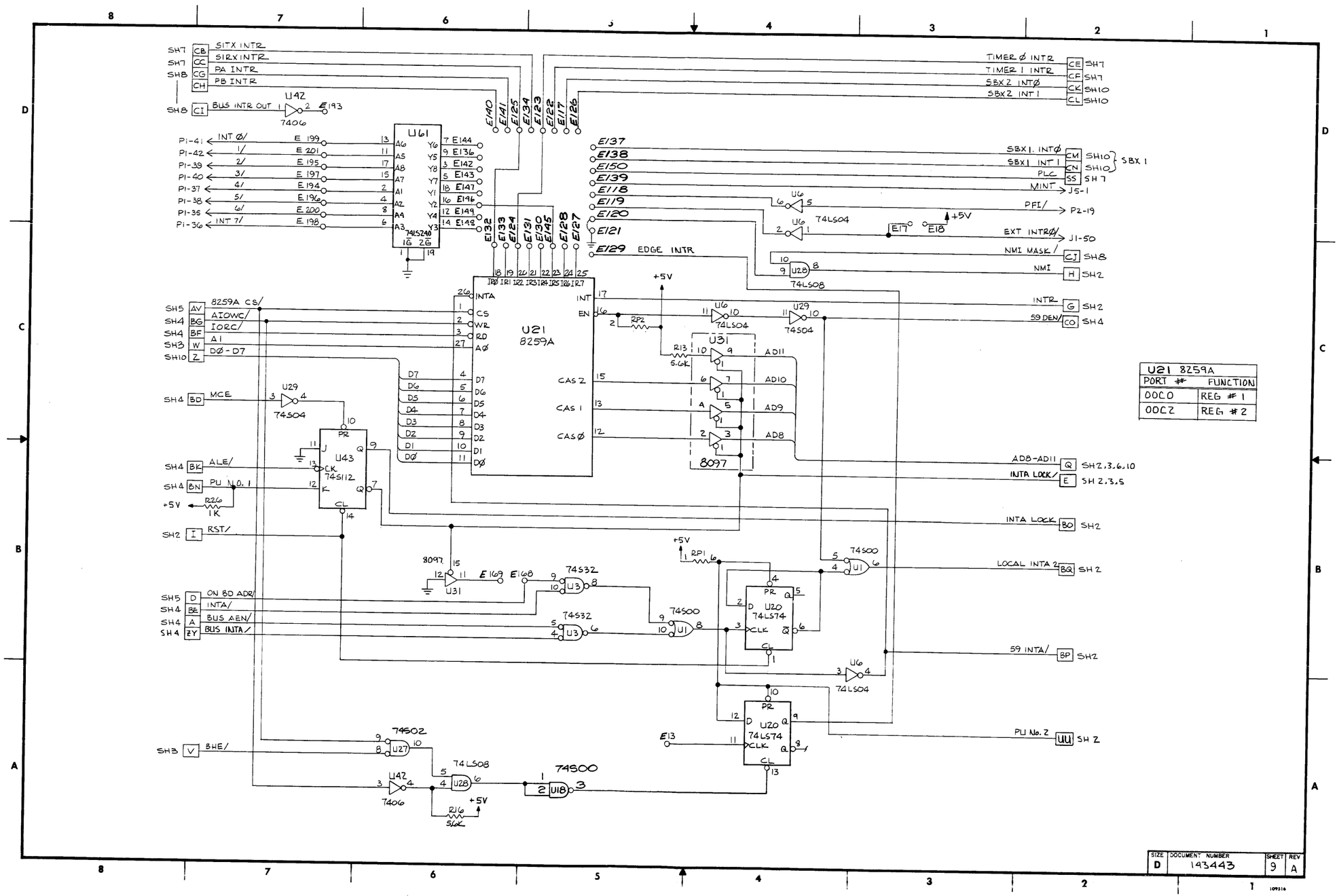
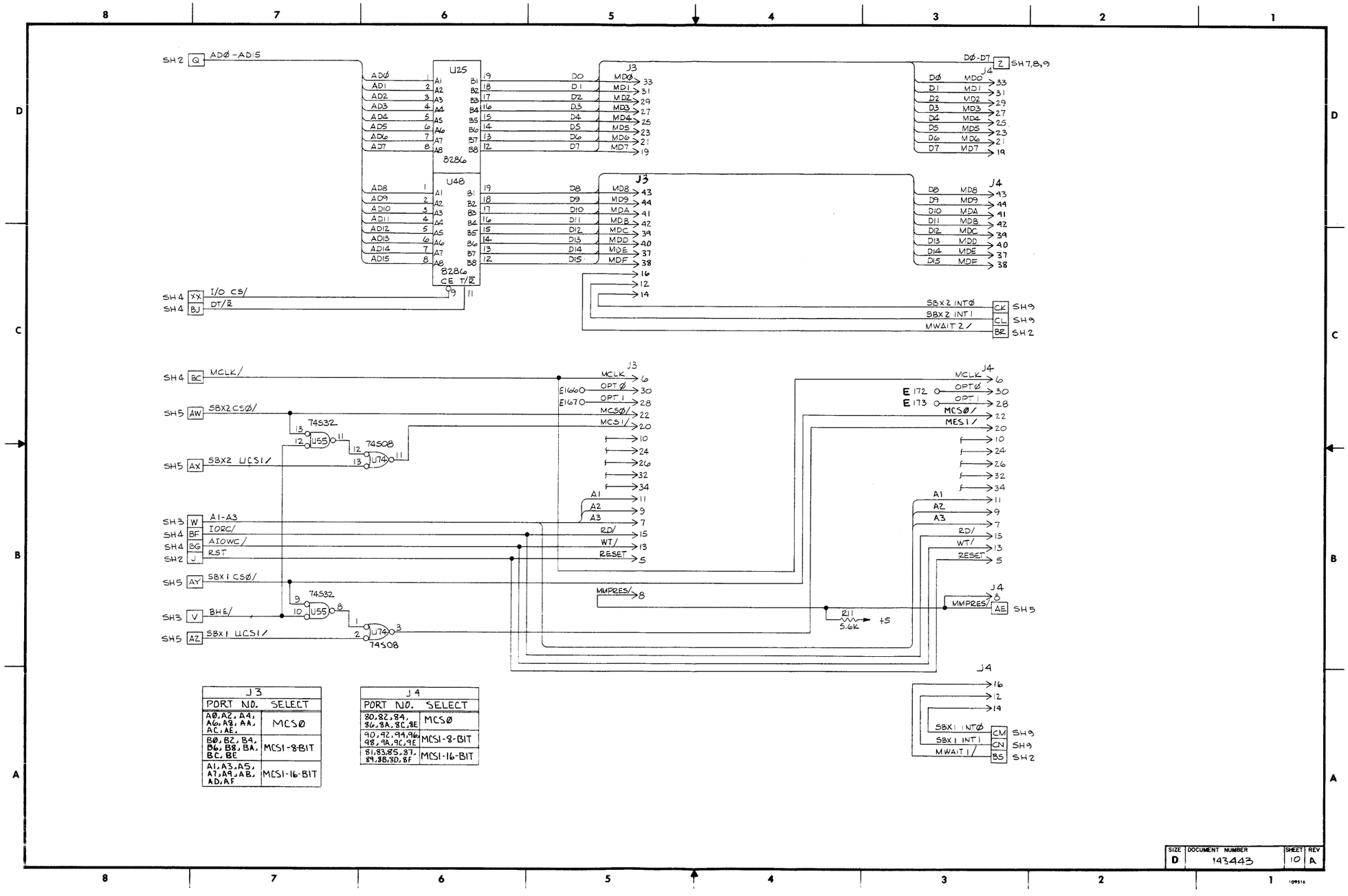


Figure 5-3. iSBC 86/05™ Board Schematic Diagram (Sheet 9 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.



J3	
PORT NO.	SELECT
A0, A2, A4, A6, A8, AA, AC, AE.	MCS0
B0, B2, B4, B6, B8, BA, BC, BE	MCS1-8-BIT
A1, A3, A5, A7, A9, AB, AD, AF	MCS1-16-BIT

J4	
PORT NO.	SELECT
80, 82, 84, 86, 88, 8A, 8C, 8E	MCS0
90, 92, 94, 96, 98, 9A, 9C, 9E	MCS1-8-BIT
81, 83, 85, 87, 89, 8B, 8D, 8F	MCS1-16-BIT

SIZE	DOCUMENT NUMBER	SHEET	REV
D	143443	10	A

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-3. iSBC 86/05™ Board Schematic Diagram (Sheet 10 of 10)

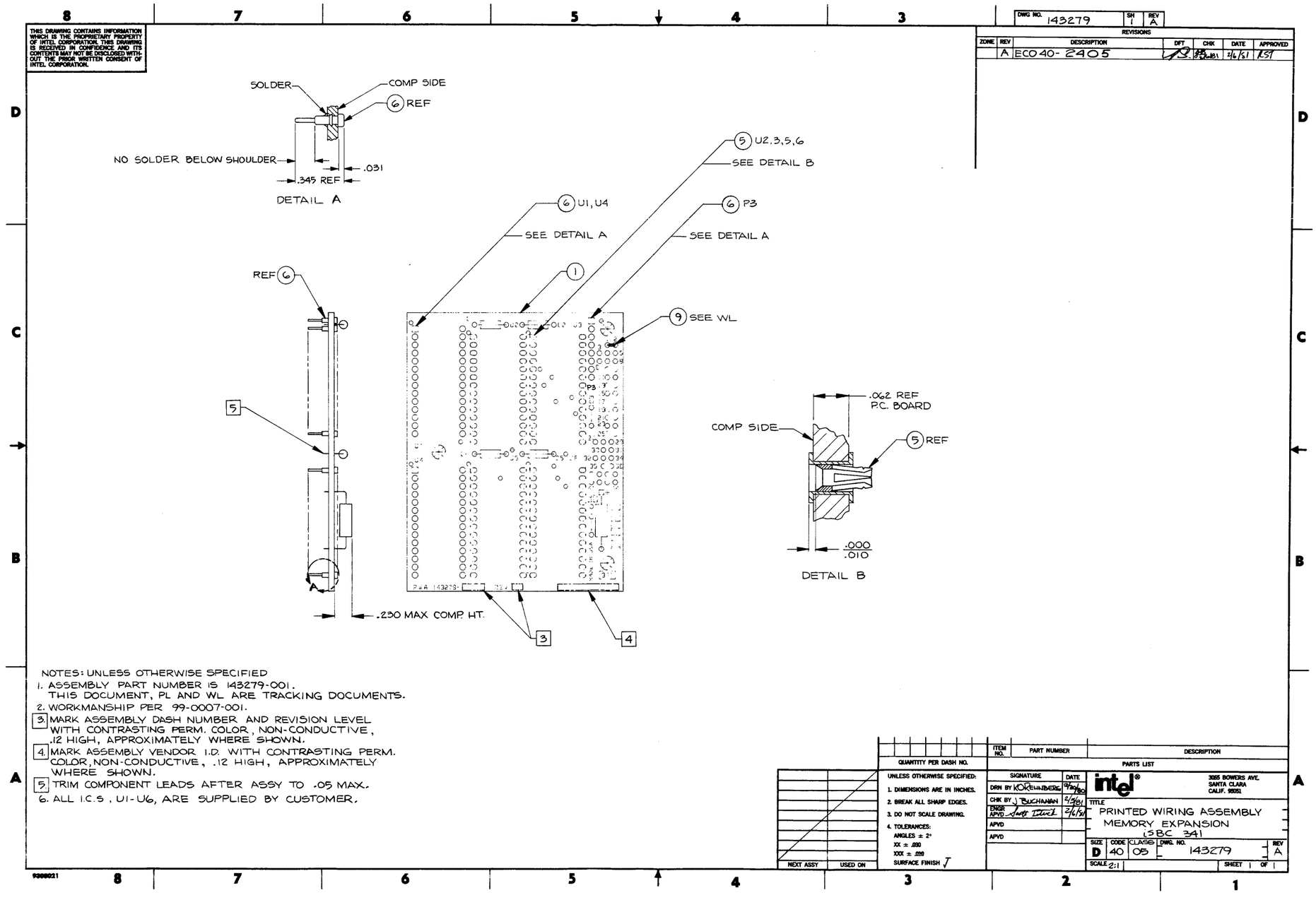
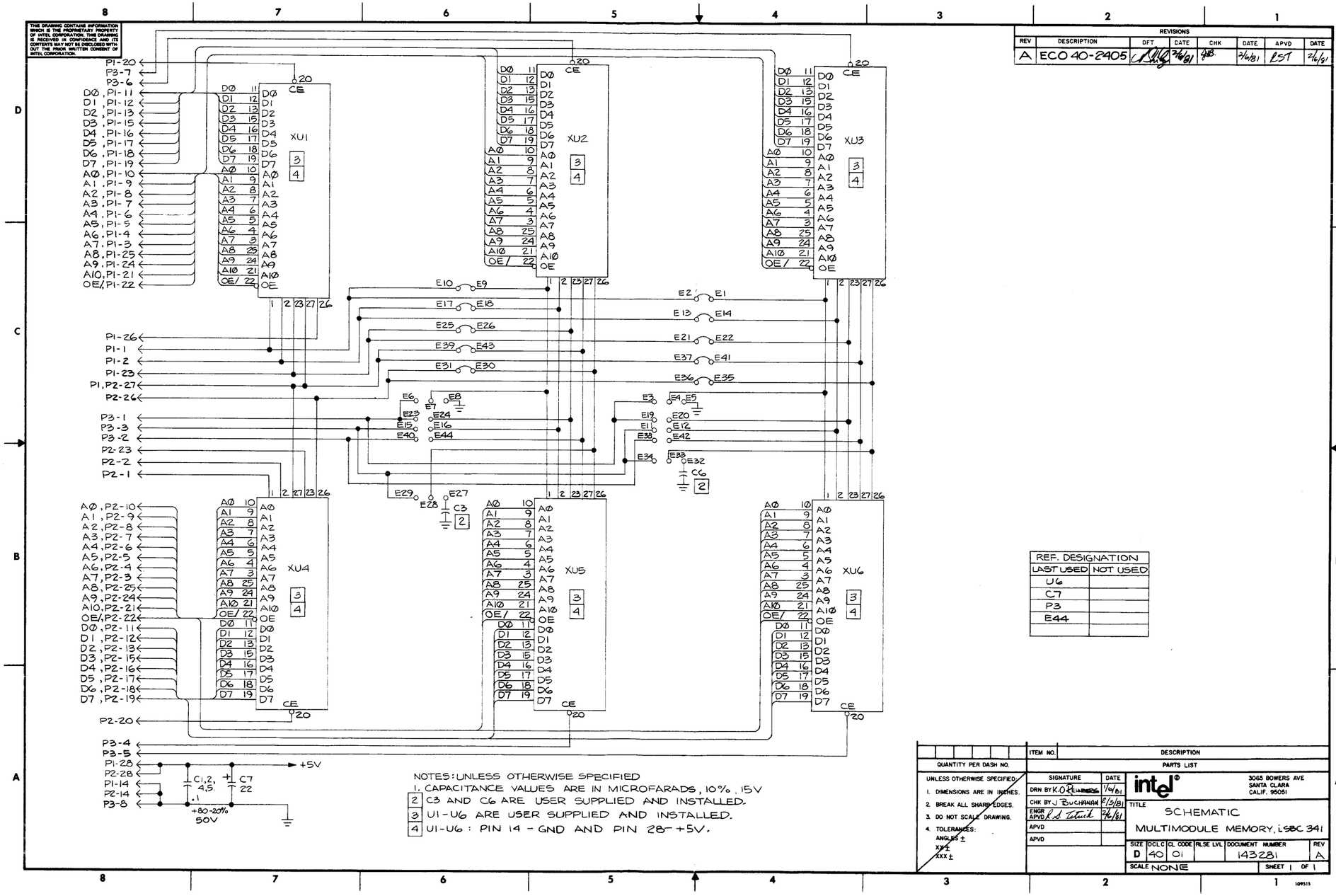


Figure 5-4. iSBC 341™ ROM Expansion Module Parts Location Drawing

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.



CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-5. iSBC 341™ ROM Expansion Module Schematic Diagram

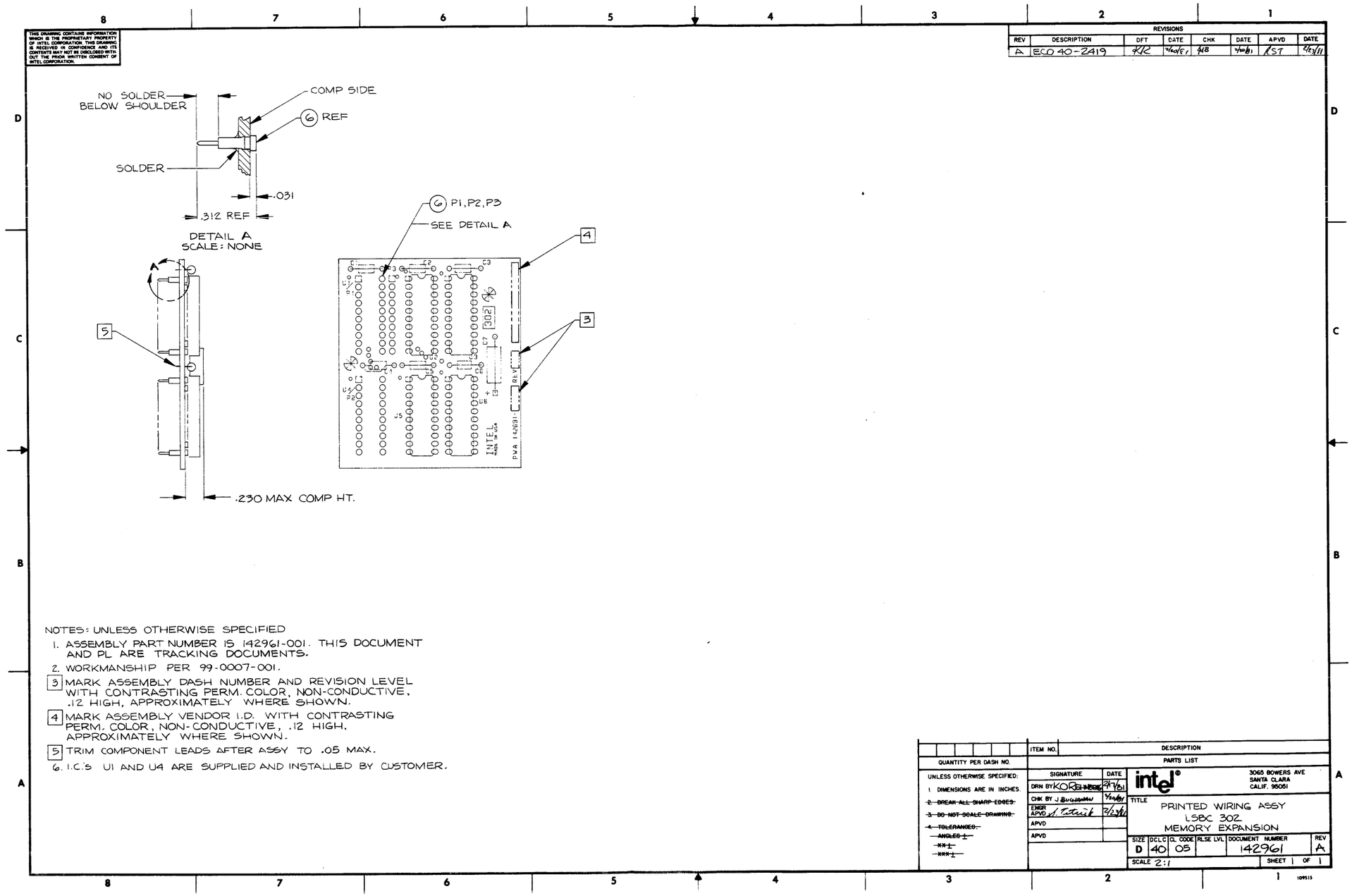


Figure 5-6. iSBC 302™ RAM Expansion Module Parts Location Drawing

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

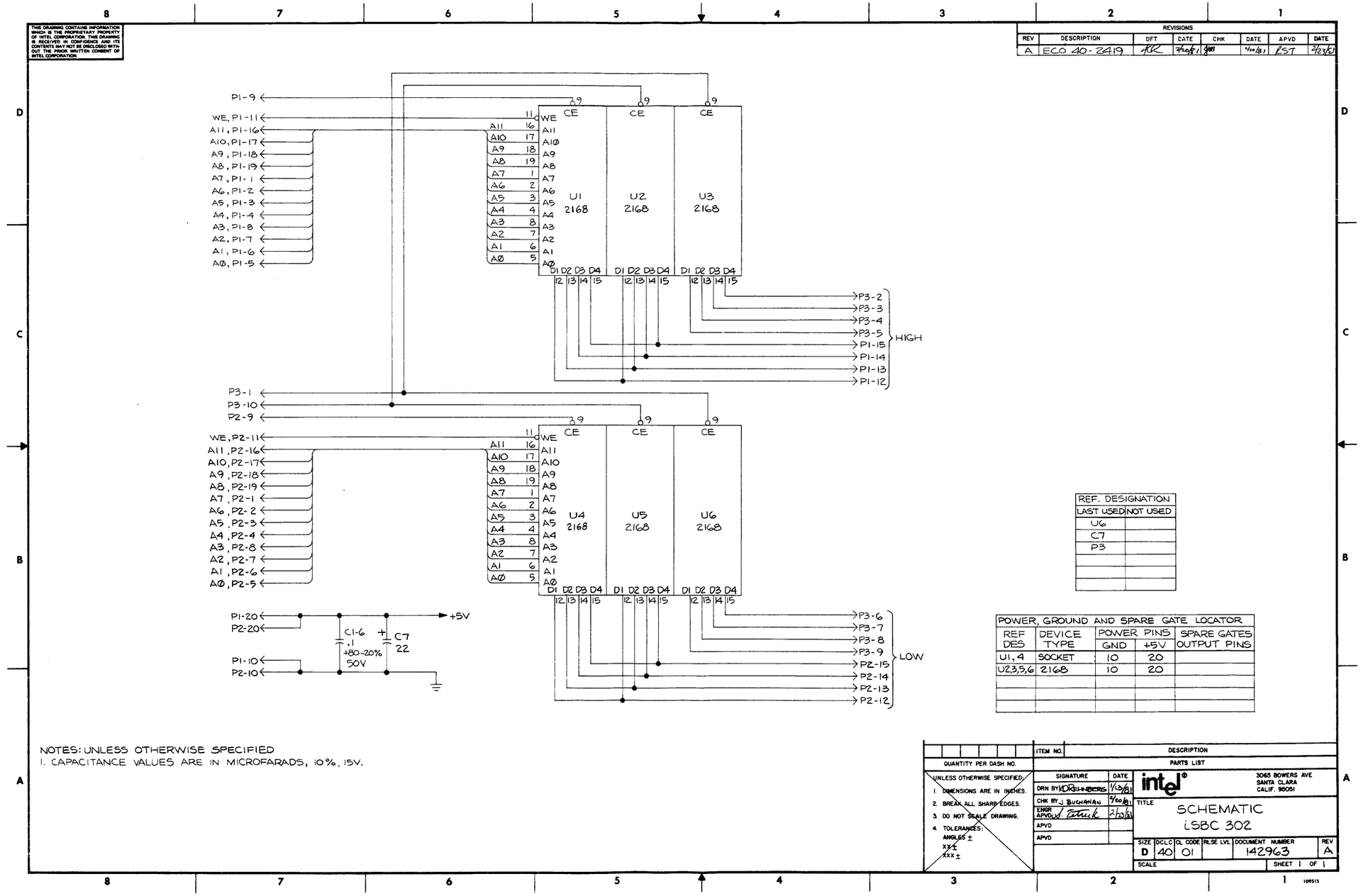


Figure 5-7. iSBC 302™ RAM Expansion Module Schematic Diagram

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

APPENDIX A
TELETYPEWRITER MODIFICATIONS

A-1. INTRODUCTION

This appendix provides information required to modify a Model ASR-33 Teletypewriter for use with certain Intel iSBC 80 computer systems.

A-2. INTERNAL MODIFICATIONS

WARNING

Hazardous voltages are exposed when the top cover of the teletypewriter is removed. To prevent accidental shock, disconnect the teleprinter power cord before proceeding beyond this point.

Remove the top cover and modify the teletypewriter as follows:

a. Remove blue lead from 750-ohm tap on current source resistor, reconnect this lead to 1450-ohm tap. (Refer to figures A-1 and A-2.)

b. On terminal block, change two wires as follows to create an internal full-duplex loop (refer to figures A-1 and A-3):

   1. Remove brown/yellow lead from terminal 3; reconnect this lead to terminal 5.
   2. Remove white/blue lead from terminal 4; reconnect this lead to terminal 5.

c. On terminal block, remove violet lead from terminal 8; reconnect this lead to terminal 9. This changes the receiver current level from 60 mA to 20 mA.

A relay circuit card must be fabricated and connected to the paper tape reader drive circuit. The relay circuit card to be fabricated requires a relay, a diode, a thyractor, a small 'vector' board for mounting the components, and suitable hardware for mounting the assembled relay card.

A circuit diagram of the relay circuit card is included in figure A-4; this diagram also includes the part numbers of the relay, diode, and thyractor. (Note that a 470-ohm resistor and a 0.1 F capacitor may be substituted for the thyractor.) After the relay circuit card has been assembled, mount it in position as shown in figure A-5. Secure the card to the base plate using two self-tapping screws. Connect the relay circuit to the distributor trip magnet and mode switch as follows:

a. Refer to figure A-4 and connect a wire (Wire 'A') from relay circuit card to terminal L2 on mode switch. (See figure A-6.)

b. Disconnect brown wire shown in figure A-7 from plastic connector. Connect this brown wire to terminal L2 on mode switch. (Brown wire will have to be extended.)

c. Refer to figure A-4 and connect a wire (Wire 'B') from relay circuit board to terminal L1 on mode switch.

A-3. EXTERNAL CONNECTIONS

Connect a two-wire receive loop, a two-wire send loop, and a two-wire tape reader control loop to the external device as shown in figure A-4. The external connector pin numbers shown in figure A-4 are for interface with an RS232C device.

A-4. iSBC 530 TTY ADAPTER

The iSBC 530 TTY adapter, which converts RS232C signal levels to an optically isolated 20 mA current loop interface, provides signal translation for transmitted data, received data, and a paper tape reader relay. The iSBC 530 TTY adapter interfaces an Intel iSBC 80 computer system to a teletypewriter as shown in figure A–8.

The iSBC 530 TTY adapter requires +12V at 98 mA and –12V at 98 mA. An auxiliary supply must be used if the iSBC 80 system does not supply this power. A schematic diagram of the iSBC 530 TTY adapter is supplied with the unit. The following auxiliary power connector (or equivalent) must be procured by the user:

Connector, Molex 09-50-7071
Pins, Molex 08-50-0106
Polarizing Key, Molex 15-04-0219

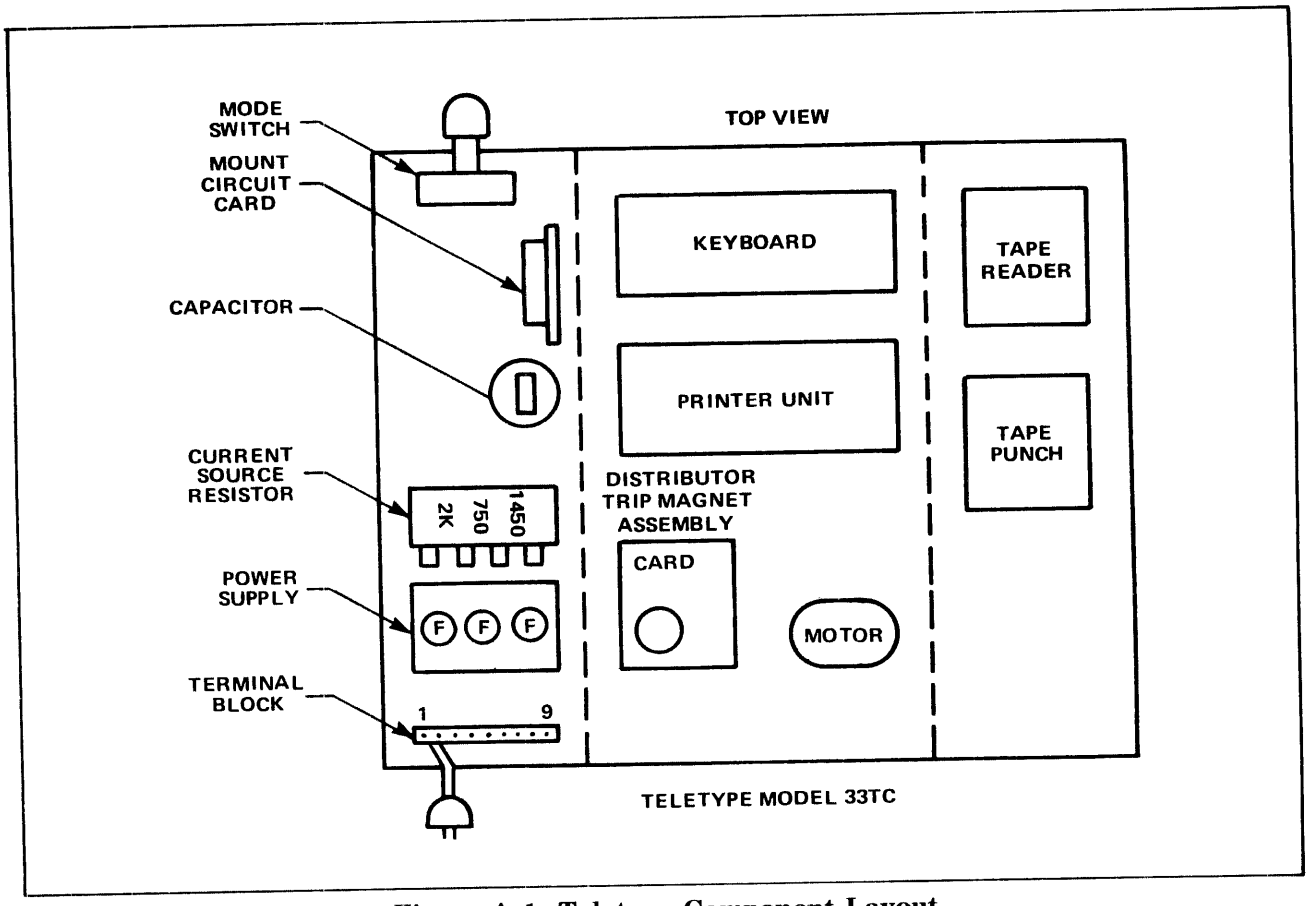


Figure A-1. Teletype Component Layout

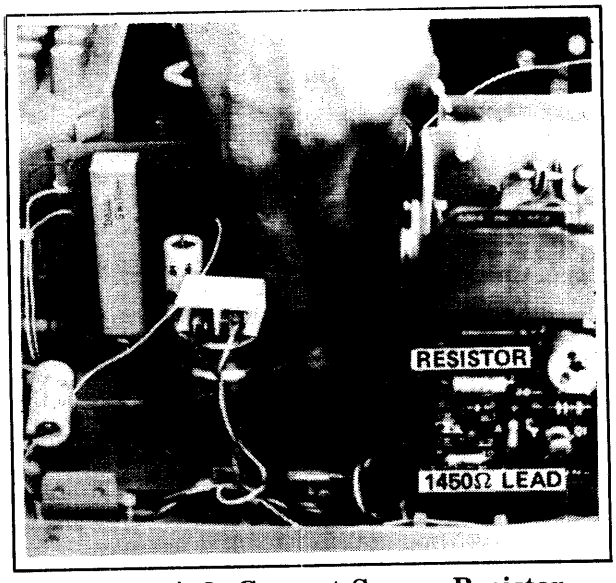


Figure A-2. Current Source Resistor

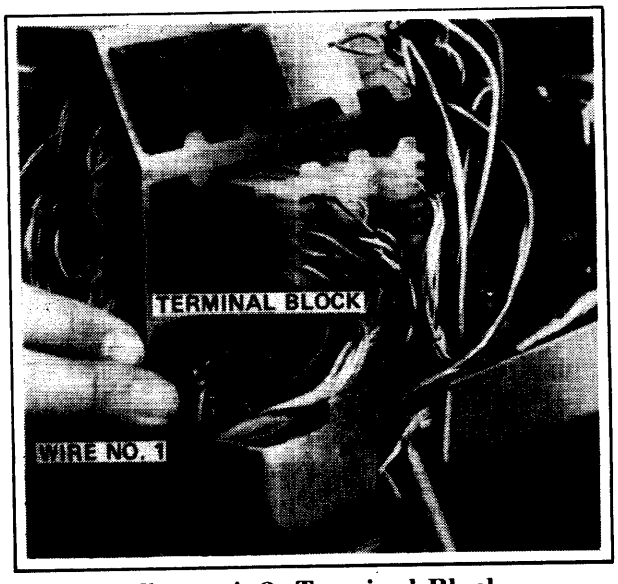


Figure A-3. Terminal Block

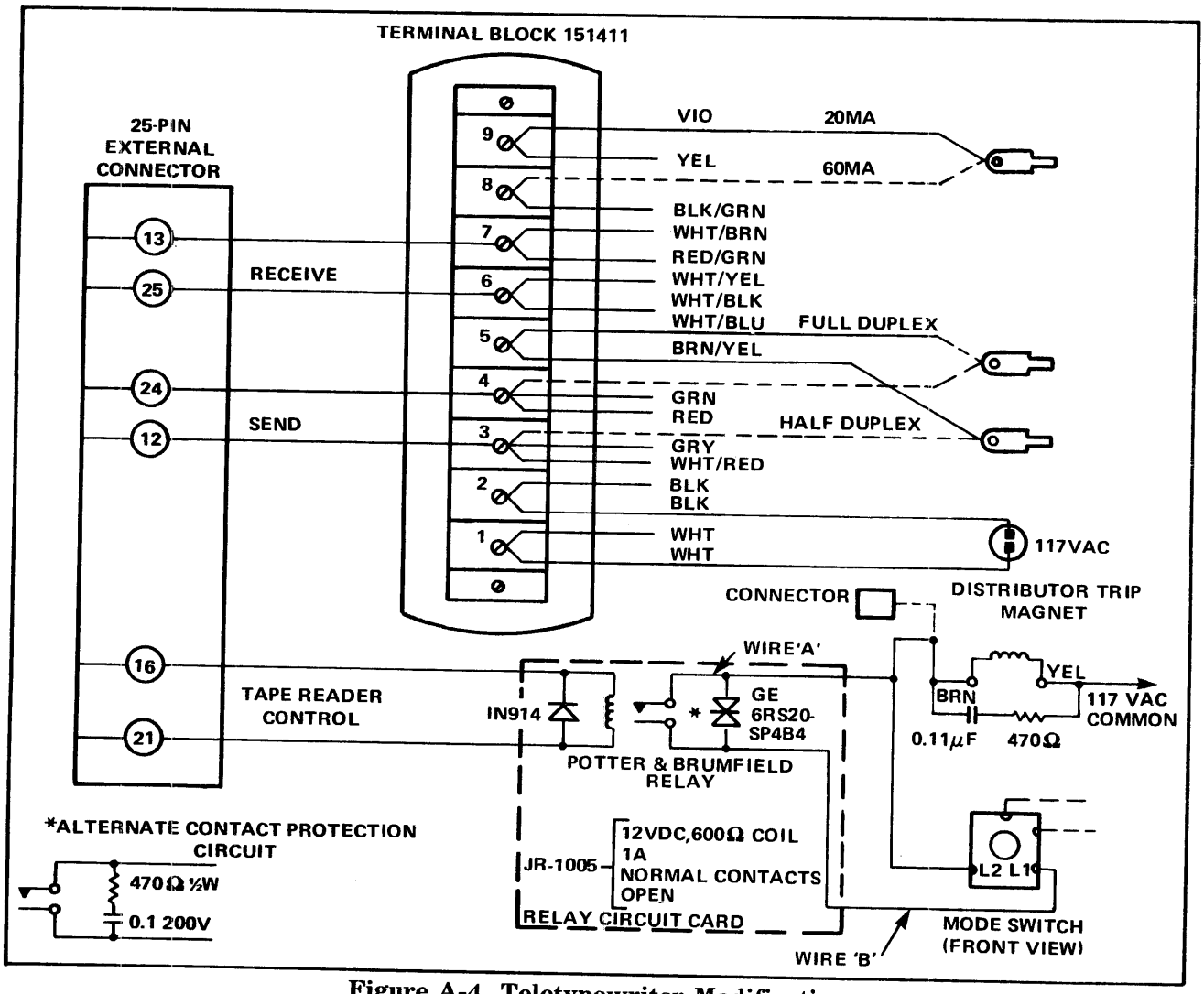


Figure A-4. Teletypewriter Modifications

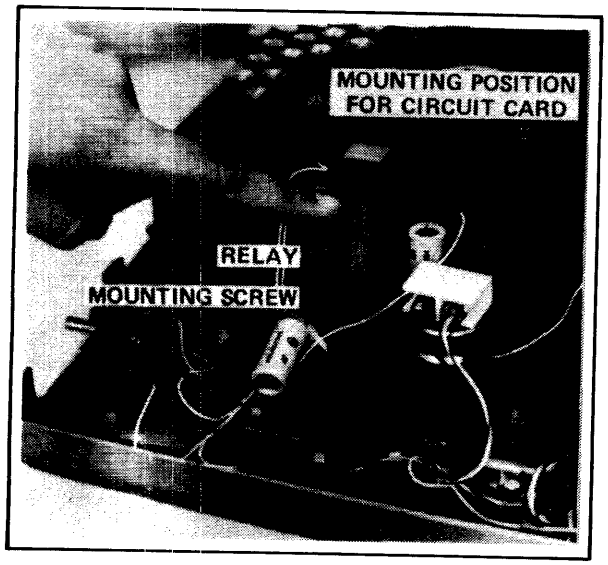


Figure A-5. Relay Circuit

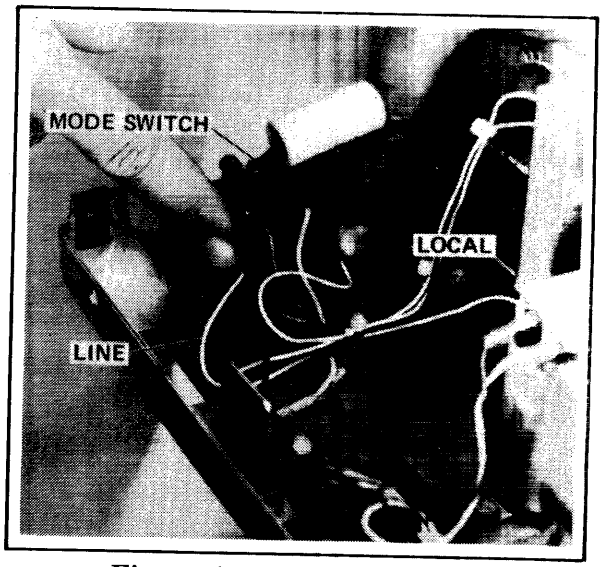


Figure A-6. Mode Switch

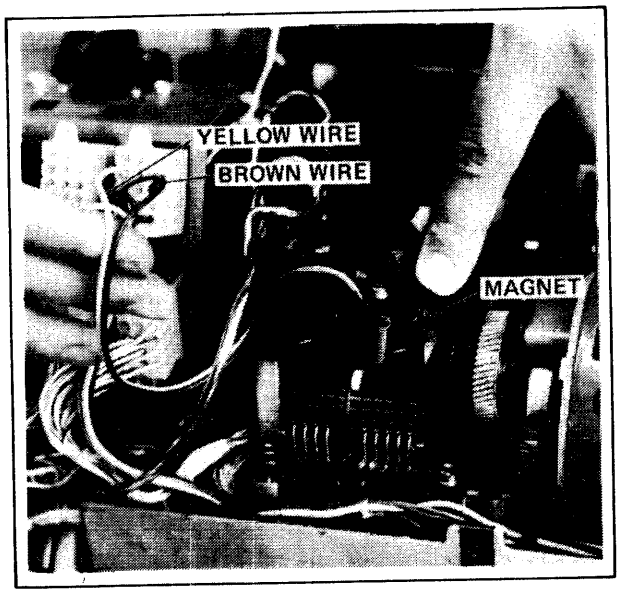


Figure A-7. Distributor Trip Magnet

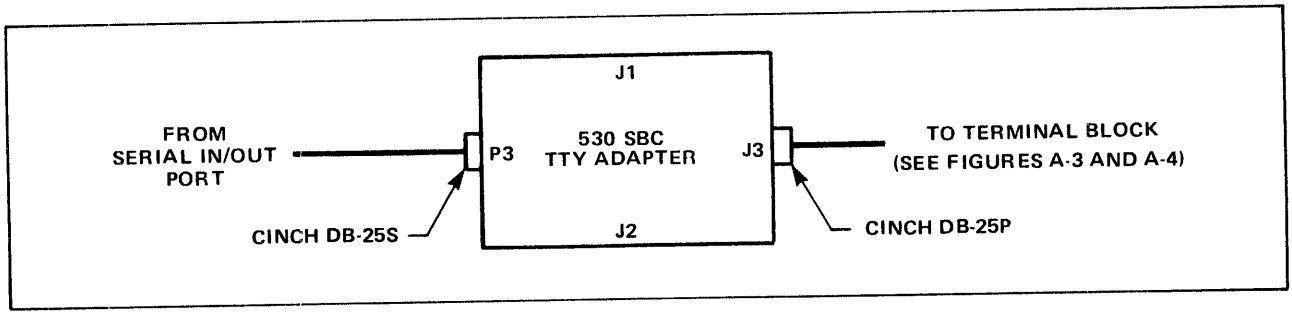


Figure A-8. TTY Adapter Cabling

APPENDIX B
DECODE PROM MEMORY MAPS

MEMORY DECODE PROM (U73)

The iSBC 86/05 board utilizes one Intel pre-programmed PROM in the memory decode circuitry. Decode PROM operation is discussed in sections 4-5 and 4-6 of the text. Table B-1 is the PROM memory map for the memory decode PROM.

I/O DECODE PROM (U72)

The iSBC 86/05 board utilizes one Intel pre-programmed PROM in the I/O decode circuitry. Decode PROM operation is discussed in sections 4-5 and 4-7 of the text. Table B-2 is the PROM memory map for the I/O decode PROM.

Table B-1. Memory Decode PROM (U73) Map
Part No. 143636-001

000	04	04	04	04	04	04	04	04	04	04	04	04	04	04	04	04
010	04	04	04	04	04	04	04	04	04	04	04	04	04	04	04	04
020	05	05	05	05	05	05	05	05	0F	0F	0F	0F	0F	0F	0F	0F
030	05	05	05	05	05	05	05	05	0F	0F	0F	0F	0F	0F	0F	0F
040	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
050	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
060	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
070	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
080	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
090	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
0A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
0B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
0C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
0D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
0E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
0F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
100	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
110	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
120	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
130	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
140	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
150	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
160	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
170	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
180	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
190	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F

(continued)

Table B-1. Memory Decode PROM (U73) Map
Part No. 143636-001
(Continued)

200	02	0F	0F	0F	0F	0F	0F	0F	02	0F	0F	0F	0F	0F	0F	0F
210	02	0F	0F	0F	0F	0F	0F	0F	02	0F	0F	0F	0F	0F	0F	0F
220	02	0F	0F	0F	0F	0F	0F	0F	02	0F	0F	0F	0F	0F	0F	0F
230	02	0F	0F	0F	0F	0F	0F	0F	02	0F	0F	0F	0F	0F	0F	0F
240	02	0F	0F	0F	0F	0F	0F	0F	02	0F	0F	0F	0F	0F	0F	0F
250	02	0F	0F	0F	0F	0F	0F	0F	02	0F	0F	0F	0F	0F	0F	0F
260	02	0F	0F	0F	0F	0F	0F	0F	02	0F	0F	0F	0F	0F	0F	0F
270	02	0F	0F	0F	0F	0F	0F	0F	02	0F	0F	0F	0F	0F	0F	0F
280	03	0F	0F	0F	0F	0F	0F	0F	03	0F	0F	0F	0F	0F	0F	0F
290	03	0F	0F	0F	0F	0F	0F	0F	03	0F	0F	0F	0F	0F	0F	0F
2A0	03	0F	0F	0F	0F	0F	0F	0F	03	0F	0F	0F	0F	0F	0F	0F
2B0	03	0F	0F	0F	0F	0F	0F	0F	03	0F	0F	0F	0F	0F	0F	0F
2C0	03	0F	0F	0F	0F	0F	0F	0F	03	0F	0F	0F	0F	0F	0F	0F
2D0	03	0F	0F	0F	0F	0F	0F	0F	03	0F	0F	0F	0F	0F	0F	0F
2E0	03	0F	0F	0F	0F	0F	0F	0F	03	0F	0F	0F	0F	0F	0F	0F
2F0	03	0F	0F	0F	0F	0F	0F	0F	03	0F	0F	0F	0F	0F	0F	0F
300	00	02	0F	0F	00	0F	0F	0F	00	02	0F	0F	00	0F	0F	0F
310	00	02	0F	0F	00	0F	0F	0F	00	02	0F	0F	00	0F	0F	0F
320	00	02	0F	0F	00	0F	0F	0F	00	02	0F	0F	00	0F	0F	0F
330	00	02	0F	0F	00	0F	0F	0F	00	02	0F	0F	00	0F	0F	0F
340	00	03	0F	0F	00	0F	0F	0F	00	03	0F	0F	00	0F	0F	0F
350	00	03	0F	0F	00	0F	0F	0F	00	03	0F	0F	00	0F	0F	0F
360	00	03	0F	0F	00	0F	0F	0F	00	03	0F	0F	00	0F	0F	0F
370	00	03	0F	0F	00	0F	0F	0F	00	03	0F	0F	00	0F	0F	0F
380	01	00	02	0F	01	00	0F	0F	01	00	02	0F	01	00	0F	0F
390	01	00	02	0F	01	00	0F	0F	01	00	02	0F	01	00	0F	0F
3A0	01	00	03	0F	01	00	0F	0F	01	00	03	0F	01	00	0F	0F
3B0	01	00	03	0F	01	00	0F	0F	01	00	03	0F	01	00	0F	0F
3C0	01	01	00	02	01	01	00	0F	01	01	00	02	01	01	00	0F
3D0	01	01	00	03	01	01	00	0F	01	01	00	03	01	01	00	0F
3E0	01	01	01	00	01	01	01	00	01	01	01	00	01	01	01	00
3F0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01

Table B-2. I/O Decode PROM (U72) Map
Part No. 143635-001

000	06	0F	06	0F	06	0F	06	0F	06	0F	06	0F	06	0F	06	0F
010	06	0F	06	0F	06	0F	06	0F	06	0F	06	0F	06	0F	06	0F
020	06	0F	06	0F	07	0F	07	0F	06	0F	06	0F	07	0F	07	0F
030	06	0F	06	0F	07	0F	07	0F	06	0F	06	0F	07	0F	07	0F
040	04	0F	04	0F	0F	0F	0F	0F	0F	0F	0F	0F	04	0F	04	0F
050	04	0F	04	0F	0F	0F	0F	0F	0F	0F	0F	0F	04	0F	04	0F
060	04	0F	04	0F	0F	0F	0F	0F	0F	0F	0F	0F	05	0F	05	0F
070	04	0F	04	0F	0F	0F	0F	0F	0F	0F	0F	0F	05	0F	05	0F
080	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03
090	02	02	02	02	02	02	02	02	02	02	02	02	02	02	02	02
0A0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
0B0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
0D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
0E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
0F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
100	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
110	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
120	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
130	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
140	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
150	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
160	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
170	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
180	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
190	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
1F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F

(Continued)

Table B-2. I/O Decode PROM (U72) Map
Part No. 143635-001
(Continued)

200	07	0F	07	0F	0F	0F	0F	0F	07	0F	07	0F	0F	0F	0F	0F
210	07	0F	07	0F	0F	0F	0F	0F	07	0F	07	0F	0F	0F	0F	0F
220	07	0F	07	0F	0F	0F	0F	0F	07	0F	07	0F	0F	0F	0F	0F
230	07	0F	07	0F	0F	0F	0F	0F	07	0F	07	0F	0F	0F	0F	0F
240	05	0F	05	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
250	05	0F	05	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
260	05	0F	05	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
270	05	0F	05	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
280	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
290	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
2A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
2B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
2C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
2D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
2E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
2F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
300	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
310	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
320	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
330	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
340	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
350	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
360	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
370	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
380	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
390	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
3A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
3B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
3C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
3D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
3E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
3F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F

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